MT6351 PMIC Datasheet

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Document Revision History

Revision	Date	Author	Description
1.0	2015-11-26	Stephen Chou	First release
1.1	2016-01-13	Stephen Chou	Add MT6351V/DV information
1.2	2016-09-12	Stephen Chou	Modify AVDD18_AUD(K3)Pin Voltage Range (Page17)

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.7 ~ 4.8V
- 8 buck converters and 31 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- Flexibility for various configurations of indicator LED current source: 4 ISINK
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver 1.1/1.2 (BC1.x) Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 199-pin MFC VFBGA package

1.2 Applications

MT6351 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

MT6351V is for MT6755/MT6797 series.
MT6351DV is for MT6757 series.

1.3 General Descriptions

MT6351 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 8 buck converters and 31 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

LED drivers support up to 4 channels of LEDs with independent control. Flexible control includes register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6351 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6351 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6351 is available in a 199-pin MFC VFBGA package. The operating temperature ranges from -20 to +85°C.

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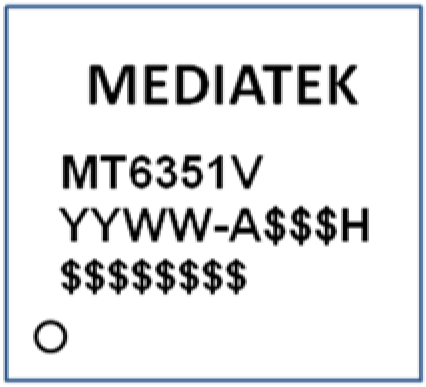
1.4 Ordering Information

Order #	Marking	Temp. range	Package	Note
MT6351V/A		-20 ~ +85°C	MFC VFBGA 199L	For MT6755/MT6797 series
MT6351DV/A		-20 ~ +85°C	MFC VFBGA 199L	For MT6757 series

1.5 Top Marking Definition

MT6351V/A



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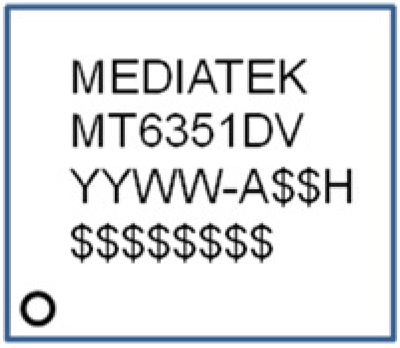
MT6351DV/A



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1.6 Pin Assignments and Descriptions

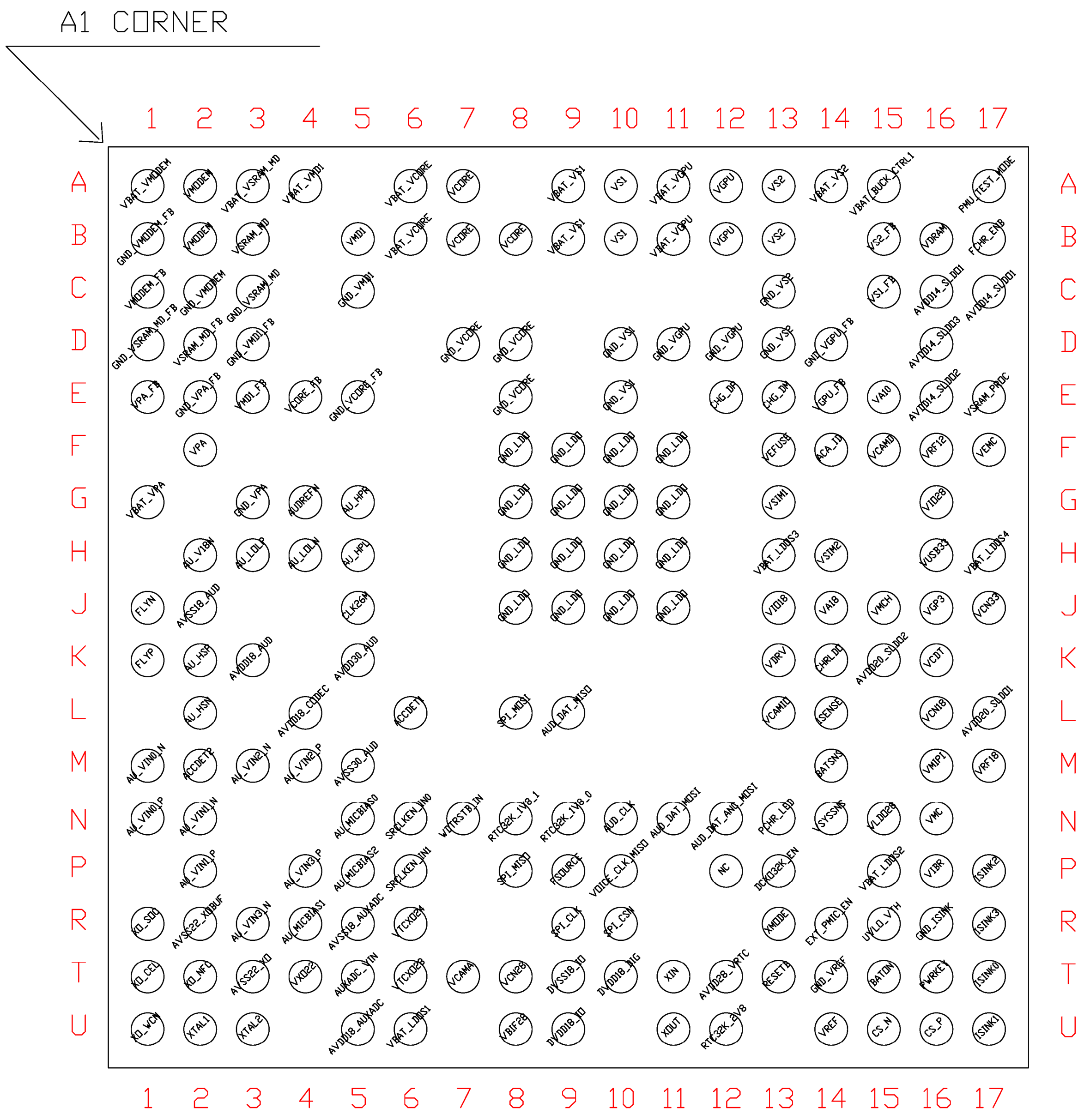

Figure 1-1. MT6351 MFC VFBGA 199 (7x7mm) pin assignment

Table 1-1. MT6351 pin descriptions

Ball	Symbol	I/O	Description
A6, B6	VBAT_VCORE	PWR	Power supply of VCORE
B7, B8, A7	VCORE	O	SW node of VCORE
D7, D8, E8	GND_VCORE	GND	VCORE ground
E4	VCORE_FB	I	BUCK VCORE feedback pin
E5	GND_VCORE_FB	I	Remote sense on ground of VCORE

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Ball	Symbol	I/O	Description
A11, B11	VBAT_VGPU	PWR	Power supply of VGPU
A12, B12	VGPU	O	SW node of VGPU
D11, D12	GND_VGPU	GND	VGPU ground
E14	VGPU_FB	I	BUCK VGPU feedback pin
D14	GND_VGPU_FB	I	Remote sense on ground of VGPU
A1	VBAT_VMODEM	PWR	Power supply of VMODEM
A2, B2	VMODEM	O	SW node of VMODEM
C2	GND_VMODEM	GND	VMODEM ground
C1	VMODEM_FB	I	BUCK VMODEM feedback pin
B1	GND_VMODEM_FB	I	Remote sense on ground of VMODEM
A4	VBAT_VMD1	PWR	Power supply of VMD1
B5	VMD1	O	SW node of VMD1
C5	GND_VMD1	GND	VMD1 ground
E3	VMD1_FB	I	BUCK VMD1 feedback pin
D3	GND_VMD1_FB	I	Remote sense on ground of VMD1
A3	VBAT_VSRAM_MD	PWR	Power supply of VSRAM_MD
B3	VSRAM_MD	O	SW node of VSRAM_MD
C3	GND_VSRAM_MD	GND	VSRAM_MD ground
D2	VSRAM_MD_FB	I	BUCK VSRAM_MD feedback pin
D1	GND_VSRAM_MD_FB	I	Remote sense on ground of VSRAM_MD
A9, B9	VBAT_VS1	PWR	Power supply of VS1
A10, B10	VS1	O	SW node of VS1
D10, E10	GND_VS1	GND	VS1 ground
C15	VS1_FB	I	BUCK VS1 feedback pin
G1	VBAT_VPA	PWR	Power supply of VPA
F2	VPA	O	SW node of VPA
G3	GND_VPA	GND	VPA ground
E1	VPA_FB	I	BUCK VPA feedback pin
E2	GND_VPA_FB	I	Remote sense on ground of VPA
A14	VBAT_VS2	PWR	Power supply of VS2
A13, B13	VS2	O	SW node of VS2
C13, D13	GND_VS2	GND	VS2 ground
B15	VS2_FB	I	BUCK VS2 feedback pin
A15	VBAT_BUCK_CTRL1	PWR	Power supply of buck controller
T6	VTCXO28	O	VTCXO28 output voltage
R6	VTCXO24	O	VTCXO24 output voltage
M17	VRF18	O	VRF18 output voltage
J17	VCN33	O	VCN33 output voltage
T8	VCN28	O	VCN28 output voltage
L16	VCN18	O	VCN18 output voltage
T7	VCAMA	O	VCAMA output voltage
L13	VCAMIO	O	VCAMIO output voltage
N15	VLDO28	O	VLDO28 output voltage
F15	VCAMD	O	VCAMD output voltage
E15	VA10	O	VA10 output voltage
J14	VA18	O	VA18 output voltage

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Ball	Symbol	I/O	Description
E17	VSRAM_PROC	O	VSRAM_PROC output voltage
G13	VSIM1	O	VSIM1 output voltage
H14	VSIM2	O	VSIM2 output voltage
M16	VMIPI	O	VMIPI output voltage
J16	VGP3	O	VGP3 output voltage
F13	VEFUSE	O	VEFUSE output voltage
G16	VIO28	O	VIO28 output voltage
N16	VMC	O	VMC output voltage
J15	VMCH	O	VMCH output voltage
F17	VEMC	O	VEMC output voltage
P16	VIBR	O	VIBR output voltage
H16	VUSB33	O	VUSB33 output voltage
U8	VBIF28	O	VBIF28 output voltage
J13	VIO18	O	VIO18 output voltage
T12	AVDD28_VRTC	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
T10	DVDD18_DIG	O	VDIG18 output voltage
F16	VRF12	O	VRF12 output voltage
B16	VDRAM	O	VDRAM output voltage
T4	VXO22	O	VDCXO output voltage
T9	DVSS18_IO	GND	Digital IO GND
U9	DVDD18_IO	PWR	Digital IO power
U6	VBAT_LDOS1	PWR	Power supply input of LDO group 1
P15	VBAT_LDOS2	PWR	Power supply input of LDO group 2
H13	VBAT_LDOS3	PWR	Power supply input of LDO group 3
H17	VBAT_LDOS4	PWR	Power supply input of LDO group 4
C16, C17	AVDD14_SLDO1	PWR	1.35V power supply of SLDO1
E16	AVDD14_SLDO2	PWR	1.35V power supply of SLDO2
D16	AVDD14_SLDO3	PWR	1.35V power supply of SLDO3
L17	AVDD20_SLDO1	PWR	2V power supply of SLDO1
K15	AVDD20_SLDO2	PWR	2V power supply of SLDO2
K13	VDRV	O	Charger current drive output
K16	VCDT	I	Fractional charger input voltage for charger detection
E13	CHG_DM	I	USB D- for BC1.1 standard
E12	CHG_DP	I	USB D+ for BC1.1 standard
K14	CHRLDO	O	CHRLDO output voltage
L14	ISENSE	I	Positive terminal for battery's charging current sensing resistor
M14	BATSNS	I	Negative terminal for battery's charging current sensing resistor
F14	ACA_ID	I	BC1.1 ACA detection pin
B17	FCHR_ENB	I	Force charging disable pin (merged with HOMEKEY; same as MT6323)
T15	BATON	I	Battery NTC pin for battery and its temperature sensing
R15	UVLO_VTH	I	UVLO threshold control pin

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Ball	Symbol	I/O	Description
U15	CS_N	I	Fuel gauge ADC input pin
U16	CS_P	I	Fuel gauge ADC input pin
T17	ISINK0	I	ISINK channel 0
U17	ISINK1	I	ISINK channel 1
P17	ISINK2	I	ISINK channel 2
R17	ISINK3	I	ISINK channel 3
N13	PCHR_LED	I	Pre-Charge Indicator
R16	GND_ISINK	GND	ISINK ground
N9	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
N8	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
U12	RTC32K_2V8	O	VRTC domain 32kHz clock output
T11	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
U11	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
R9	SPI_CLK	I	SPI control interface
R10	SPI_CSN	IO	SPI control interface
P8	SPI_MISO	IO	SPI control interface
L8	SPI_MOSI	IO	SPI control interface
N7	WDTRSTB_IN	I	Watchdog reset from AP
T13	RESETB	O	System reset release signal
N6	SRCLKEN_IN0	I	Source clock enable pin 0
P6	SRCLKEN_IN1	I	Source clock enable pin 1
R14	EXT_PMIC_EN	IO	Ext chip MT6311/MT6313 enable pin
U14	VREF	O	Bandgap reference voltage
T14	GND_VREF	GND	Ground for bandgap
N14	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
P9	FSOURCE	PWR	EFUSE power source
A17	PMU_TEST_MODE	I	PMU test mode signal (tied to GND in normal operation)
T16	PWRKEY	I	PWRKEY button
T5	AUXADC_VIN	I	AUXADC input
U5	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
R5	AVSS18_AUXADC	GND	AUXADC ground
P10	VOICE_CLK_MISO	IO	Voice wakeup control pin
L6	ACCDET1	I	Accessory detection input 1
M2	ACCDET2	I	Accessory detection input 2
J1	FLYN	O	Flying capacitor bottom
K1	FLYP	O	Flying capacitor top
N5	AU_MICBIAS0	O	Microphone Bias 0
R4	AU_MICBIAS1	O	Microphone Bias 1
P5	AU_MICBIAS2	O	Microphone Bias 2
G4	AUDREFN	GND	Audio reference ground
M1	AU_VIN0_N	I	Microphone channel 0 negative input
N1	AU_VIN0_P	I	Microphone channel 0 positive input
N2	AU_VIN1_N	I	Microphone channel 1 negative input

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Ball	Symbol	I/O	Description
P2	AU_VIN1_P	I	Microphone channel 1 positive input
M3	AU_VIN2_N	I	Microphone channel 2 negative input
M4	AU_VIN2_P	I	Microphone channel 2 positive input
R3	AU_VIN3_N	I	Microphone channel 3 negative input
P4	AU_VIN3_P	I	Microphone channel 3 positive input
N10	AUD_CLK	I	Audio control interface
L9	AUD_DAT_MISO	IO	Audio control interface
N11	AUD_DAT_MOSI	IO	Audio control interface
N12	AUD_DAT_ANC_MOSI	IO	Audio ANC control interface
K3	AVDD18_AUD	PWR	1.8V power supply of Audio
K5	AVDD30_AUD	PWR	Power supply of Audio UL
J2	AVSS18_AUD	GND	Audio DL ground
H2	AU_V18N	PWR	Audio -1.8V supply
M5	AVSS30_AUD	GND	Audio UL ground
J5	CLK26M	I	26MHz clock input
H5	AU_HPL	O	Earphone left channel output
G5	AU_HPR	O	Earphone right channel output
L2	AU_HSN	O	Handset negative output
K2	AU_HSP	O	Handset positive output
L4	AVDD18_CODEC	PWR	Power supply of CODEC
H3	AU_LOLP	O	Positive output of line-out buffer
H4	AU_LOLN	O	Negative output of line-out buffer
F8, G8, H8, J8, F9, G9, H9, J9, F10, G10, H10, J10, F11, G11, H11, J11	GND_LDO	GND	LDO ground
T3	AVSS22_XO	GND	Ground for XO
R2	AVSS22_XOBUF	GND	Ground for XO
U2	XTAL1	I	XTAL input 1
U3	XTAL2	I	XTAL input 2
R1	XO_SOC	O	26MHz output to SOC
U1	XO_WCN	O	26MHz output to Conn. RF
T1	XO_CEL	O	26MHz output to Cell. RF
T2	XO_NFC	O	26MHz output to NFC
P13	DCXO32K_EN	I	Config HW pin (VRTC)
R13	XMODE	I	Config HW pin (VRTC)
P12	NC	O	Test Mode Purpose

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				4.8	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		36.42[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6351 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A6, B6	VBAT_VCORE	0~4.8	V
B7, B8, A7	VCORE	0~4.8	V
D7, D8, E8	GND_VCORE	0	V
E4	VCORE_FB	0~4.8	V
E5	GND_VCORE_FB	0	V
A11, B11	VBAT_VGPU	0~4.8	V
A12, B12	VGPU	0~4.8	V

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Ball	Symbol	Voltage range	Unit
D11, D12	GND_VGPU	0	V
E14	VGPU_FB	0~4.8	V
D14	GND_VGPU_FB	0	V
A1	VBAT_VMODEM	0~4.8	V
A2, B2	VMODEM	0~4.8	V
C2	GND_VMODEM	0	V
C1	VMODEM_FB	0~4.8	V
B1	GND_VMODEM_FB	0	V
A4	VBAT_VMD1	0~4.8	V
B5	VMD1	0~4.8	V
C5	GND_VMD1	0	V
E3	VMD1_FB	0~4.8	V
D3	GND_VMD1_FB	0	V
A3	VBAT_VSRAM_MD	0~4.8	V
B3	VSRAM_MD	0~4.8	V
C3	GND_VSRAM_MD	0	V
D2	VSRAM_MD_FB	0~4.8	V
D1	GND_VSRAM_MD_FB	0	V
A9, B9	VBAT_VS1	0~4.8	V
A10, B10	VS1	0~4.8	V
D10, E10	GND_VS1	0	V
C15	VS1_FB	0~4.8	V
G1	VBAT_VPA	0~4.8	V
F2	VPA	0~4.8	V
G3	GND_VPA	0	V
E1	VPA_FB	0~4.8	V
E2	GND_VPA_FB	0	V
A14	VBAT_VS2	0~4.8	V
A13, B13	VS2	0~4.8	V
C13, D13	GND_VS2	0	V
B15	VS2_FB	0~4.8	V
A15	VBAT_BUCK_CTRL1	0~4.8	V
T6	VTCXO28	0~4.8	V
R6	VTCXO24	0~4.8	V
M17	VRF18	0~2.1	V
J17	VCN33	0~4.8	V
T8	VCN28	0~4.8	V
L16	VCN18	0~2.1	V
T7	VCAMA	0~4.8	V
L13	VCAMIO	0~2.1	V
N15	VLDO28	0~4.8	V
F15	VCAMD	0~2.1	V
E15	VA10	0~2.1	V
J14	VA18	0~1.98	V
E17	VSRAM_PROC	0~2.1	V

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Ball	Symbol	Voltage range	Unit
G13	VSIM1	0~4.8	V
H14	VSIM2	0~4.8	V
M16	VMIPI	0~2.1	V
J16	VGP3	0~2.1	V
F13	VEFUSE	0~4.8	V
G16	VIO28	0~4.8	V
N16	VMC	0~4.8	V
J15	VMCH	0~4.8	V
F17	VEMC	0~4.8	V
P16	VIBR	0~4.8	V
H16	VUSB33	0~4.8	V
U8	VBIF28	0~4.8	V
J13	VIO18	0~2.1	V
T12	AVDD28_VRTC	0~4.8	V
T10	DVDD18_DIG	0~1.98	V
F16	VRF12	0~2.1	V
B16	VDRAM	0~2.1	V
T4	VXO22	0~2.2	V
T9	DVSS18_IO	0	V
U9	DVDD18_IO	0~1.98	V
U6	VBAT_LDOS1	0~4.8	V
P15	VBAT_LDOS2	0~4.8	V
H13	VBAT_LDOS3	0~4.8	V
H17	VBAT_LDOS4	0~4.8	V
C16, C17	AVDD14_SLDO1	0~2.1	V
E16	AVDD14_SLDO2	0~2.1	V
D16	AVDD14_SLDO3	0~2.1	V
L17	AVDD20_SLDO1	0~2.1	V
K15	AVDD20_SLDO2	0~2.1	V
K13	VDRV	0 ~ 4.8	V
K16	VCDT	0 ~ 3.08	V
E13	CHG_DM	0 ~ 3.3	V
E12	CHG_DP	0 ~ 3.3	V
K14	CHRLDO	0 ~ 3.08	V
L14	ISENSE	0 ~ 4.8	V
M14	BATSNS	0 ~ 4.8	V
F14	ACA_ID	0 ~ 3.3	V
B17	FCHR_ENB	0 ~ 4.8	V
T15	BATON	0 ~ 4.8	V
R15	UVLO_VTH	0 ~ 4.8	V
U15	CS_N	-0.1 ~ 0.1	V
U16	CS_P	-0.1 ~ 0.1	V
T17	ISINK0	0 ~ 4.8	V
U17	ISINK1	0 ~ 4.8	V
P17	ISINK2	0 ~ 4.8	V
R17	ISINK3	0 ~ 4.8	V

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Ball	Symbol	Voltage range	Unit
N13	PCHR_LED	0 ~ 4.8	V
R16	GND_ISINK	0	V
N9	RTC32K_1V8_0	0 ~ 1.98	V
N8	RTC32K_1V8_1	0 ~ 1.98	V
U12	RTC32K_2V8	0 ~ 3.08	V
T11	XIN	0 ~ 3.08	V
U11	XOUT	0 ~ 3.08	V
R9	SPI_CLK	0 ~ 1.98	V
R10	SPI_CSN	0 ~ 1.98	V
P8	SPI_MISO	0 ~ 1.98	V
L8	SPI_MOSI	0 ~ 1.98	V
N7	WDTRSTB_IN	0 ~ 1.98	V
T13	RESETB	0 ~ 1.98	V
N6	SRCLKEN_IN0	0 ~ 1.98	V
P6	SRCLKEN_IN1	0 ~ 1.98	V
R14	EXT_PMIC_EN	0 ~ 4.8	V
U14	VREF	0 ~ 1.32	V
T14	GND_VREF	0	V
N14	VSYSSNS	0 ~ 4.8	V
P9	FSOURCE	0 ~ 1.98	V
A17	PMU_TEST_MODE	0 ~ 4.8	V
T16	PWRKEY	0 ~ 4.8	V
T5	AUXADC_VIN	0 ~ 1.8	V
U5	AVDD18_AUXADC	0 ~ 1.8	V
R5	AVSS18_AUXADC	0	V
P10	VOICE_CLK_MISO	0 ~ 1.98	V
L6	ACCDET1	0 ~ 3.3	V
M2	ACCDET2	0 ~ 3.3	V
J1	FLYN	-1.98 ~ 0	V
K1	FLYP	0 ~ 1.98	V
N5	AU_MICBIAS0	0 ~ 3.3	V
R4	AU_MICBIAS1	0 ~ 3.3	V
P5	AU_MICBIAS2	0 ~ 3.3	V
G4	AUDREFN	0	V
M1	AU_VIN0_N	0 ~ 3.3	V
N1	AU_VIN0_P	0 ~ 3.3	V
N2	AU_VIN1_N	0 ~ 3.3	V
P2	AU_VIN1_P	0 ~ 3.3	V
M3	AU_VIN2_N	0 ~ 3.3	V
M4	AU_VIN2_P	0 ~ 3.3	V
R3	AU_VIN3_N	0 ~ 3.3	V
P4	AU_VIN3_P	0 ~ 3.3	V
N10	AUD_CLK	0 ~ 1.98	V
L9	AUD_DAT_MISO	0 ~ 1.98	V
N11	AUD_DAT_MOSI	0 ~ 1.98	V

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Ball	Symbol	Voltage range	Unit
N12	AUD_DAT_ANC_MOSI	0 ~ 1.98	V
K3	AVDD18_AUD	0 ~ 2.1	V
K5	AVDD30_AUD	0 ~ 3.3	V
J2	AVSS18_AUD	0	V
H2	AU_V18N	-1.98 ~ 0	V
M5	AVSS30_AUD	0	V
J5	CLK26M	0 ~ 1.98	V
H5	AU_HPL	-1.98 ~ 1.98	V
G5	AU_HPR	-1.98 ~ 1.98	V
L2	AU_HSN	-1.98 ~ 1.98	V
K2	AU_HSP	-1.98 ~ 1.98	V
L4	AVDD18_CODEC	0 ~ 1.98	V
H3	AU_LOLP	-1.98 ~ 1.98	V
H4	AU_LOLN	-1.98 ~ 1.98	V
F8, G8, H8, J8, F9, G9, H9, J9, F10, G10, H10, J10, F11, G11, H11, J11	GND_LDO	0	V
T3	AVSS22_XO	0	V
R2	AVSS22_XOBUF	0	V
U2	XTAL1	0~2.2	V
U3	XTAL2	0~2.2	V
R1	XO_SOC	0~1.21	V
U1	XO_WCN	0~1.98	V
T1	XO_CEL	0~1.98	V
T2	XO_NFC	0~1.21	V
P13	DCXO32K_EN	0~3.08	V
R13	XMODE	0~3.08	V

2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Ambient temperature (T_A)		-20		85	°C
Junction temperature (T_J)		-20		125	°C

2.5 Electrical Characteristics

VBAT = 2.7 ~ 4.8V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					

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Parameter	Conditions	Min.	Typical	Max.	Unit
Standby	Low-power mode		350	420	μA
Power down leakage current with 32K XTAL	VBAT=4.8V, Temp=25°C			85	uA
Power down leakage current without 32K XTAL(VTCXO24)	VBAT=4.8V, Temp=25°C			95	uA
Power down leakage current without 32K XTAL(VXO22)	VBAT=4.8V, Temp=25°C		250	340	uA
Under Voltage (UV)					
Under voltage falling threshold		2.5	2.7	2.9	V
Threshold voltage accuracy		-50		+50	mV
Under voltage rising threshold	R=185K~270K (w/o charger)	2.95	3.0	3.05	V
Under voltage rising threshold w/o power path	R=185K~270K (w/i charger)	2.75	2.8	2.85	V
Under voltage rising threshold with power path	R=185K~270K (w/i charger)	2.95	3.0	3.05	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay time from VMC turn on to RESETB release		32	40	48	ms
Interrupt					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY/FCHR_ENB					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		26	32	38	ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		degree
Shut-down release threshold			110		degree

2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VGPU					

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Parameter	Conditions	Min.	Typical	Max.	Unit
Turn-on overshoot	Vout=1.0V No load Cout=69uF			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=100mA		84		%
	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=400mA		85		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=1.0A		80		%
	Vbat=3.8V, Vout=1.1V, L_DCR=30mΩ I_Load=3A		60		%
Soft start	Vout=1.0V No load Cout=69uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.0A to 3A (slew rate=2A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+5.5	%
Buck – VCORE					
Turn-on overshoot	Vout=1.0V No load Cout=69uF			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=100mA		84		%
	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=400mA		85		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=1.0A		80		%
	Vbat=3.8V, Vout=1.1V, L_DCR=30mΩ I_Load=3A		60		%
Soft start	Vout=1.0V			1	ms

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Parameter	Conditions	Min.	Typical	Max.	Unit
	No load Cout=69uF				
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.0A to 3A (slew rate=2A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+5.5	%
Buck – VMODEM					
Turn-on overshoot	Vout=0.9V No load Cout=26.7uF			10	%
Short current		Imax*1.2		Imax*3	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=100mA		79		%
	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=500mA		81		%
	Vbat=3.8V, Vout=0.9V L_DCR=30mΩ I_Load=1.2A		75		%
Soft start	Vout=0.9V No load Cout=26.7uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V, Vout=0.9V IOUT = 0.6A to 1.2A (slew rate=0.6A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+5.5	%
Buck – VMD1					
Turn-on overshoot	Vout=0.9V No load Cout=26.7uF			10	%
Short current		Imax*1.2		Imax*3	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C

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Parameter	Conditions	Min.	Typical	Max.	Unit
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=100mA		79		%
	Vbat=3.8V, Vout=0.9V, L_DCR=30mΩ I_Load=500mA		81		%
	Vbat=3.8V, Vout=0.9V L_DCR=30mΩ I_Load=1.2A		75		%
Soft start	Vout=0.9V No load Cout=26.7uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V, Vout=0.9V IOUT = 0.6A to 1.2A (slew rate=0.6A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+5.5	%
Buck – VSRAM_MD					
Turn-on overshoot	Vout=1.0V No load Cout=26.7uF			10	%
Short current		Imax*1.2		Imax*3	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=100mA		79		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=500mA		81		%
	Vbat=3.8V, Vout=1.0V L_DCR=30mΩ I_Load=1.2A		75		%
Soft start	Vout=1.0V No load Cout=26.7uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V, Vout=1.0V IOUT = 0.6A to 1.2A (slew rate=0.6A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+5.5	%
Buck – VPA					
Turn-on overshoot	No load			10	%
Short current	a. Vo=0.5V~1.25V b.Vo=1.25V~3.4V		a. 0.8 b. 1.6	a. 1.05 b. 2	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.5V, L_DCR=130mΩ R_Load=50 Ω		67		%
	Vbat=3.8V, Vout=1.2V, L_DCR=130mΩ R_Load=15 Ω		80		%
	Vbat=3.8V, Vout=2.4V, L_DCR=130mΩ R_Load=13.3 Ω		89		%
	Vbat=3.8V, Vout=3.4V, L_DCR=130mΩ R_Load=12 Ω		92		%
Soft start	No load		250		us
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			50	mVp-p
	1V>(Vbat-Vout)>0.2V I_Load=0.5*Imax 20MHz measurement BW			180	mVp-p
Load transient (PWM)	Vbat=3.8V,Vout=0.5V Rload = 50 Ω to 8.3 Ω (slew rate=10mA/us)			30	mV
	Vbat=3.8V,Vout=1.5V Rload = 50 Ω to 12.5 Ω (slew rate=90mA/us)			150	mV
	Vbat=3.8V,Vout=3.4V Rload = 113 Ω to 5 Ω (slew rate=0.65A/us)			500	mV
DC accuracy	VBAT=3.1V to 4.8V Vout<1V I_Load=10mA to Imax	-20		+20	mV
	VBAT=3.1V to 4.8V Vout≧1V I_Load=10mA to Imax	-2		+2	%
Buck – VS1					
Turn-on overshoot	No load			10	%
Short current				4	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=2V,		83		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=30mΩ I_Load=50mA				
	Vbat=3.8V, Vout=2V, L_DCR=30mΩ I_Load=500mA		88		%
	Vbat=3.8V, Vout=2V, L_DCR=30mΩ I_Load=1 A		75		%
	Vbat=3.8V, Vout=2V L_DCR=30mΩ I_Load=2 A		65		%
Soft start	No load			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVp-p
Load transient (PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.8V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+3.5	%
Buck – VS2					
Turn-on overshoot	No load			10	%
Short current				4	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.4V, L_DCR=30mΩ I_Load=50mA		82		%
	Vbat=3.8V, Vout=1.4V, L_DCR=30mΩ I_Load=500mA		85		%
	Vbat=3.8V, Vout=1.4V, L_DCR=30mΩ I_Load=1A		75		%
	Vbat=3.8V, Vout=1.4V, L_DCR=30mΩ I_Load=2A		65		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVp-p
Load transient (PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1A/us)	-3.5		+3.5	%
DC accuracy	VBAT=3.1V to 4.8V	-1		+1	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
(Included Line/Load regulation @PWM)	I_Load=10mA to Imax				
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.8V I_Load=0~10mA	-1		+3.5	%

Table 2-6. LDO specifications

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
All test condition for input power range	ALDO and DLDO for VBAT range	(note#1) Min spec: max{Output Voltage +0.35V; VBAT≧3.0}		(note #1)		4.8	V
	SLDO1 for AVDD20 range	(note#2) Min spec: max{Output Voltage +0.15V; AVDD20≧2*0.95}		(note #2)		2*1.05	V
	SLDO2 for AVDD14 range	(note#3) Min spec: max{Output Voltage +0.1V; AVDD14≧1.35*0.95}		(note #3)		1.35*1.05	V
Overall DC voltage accuracy	VXO22,VCN28, VCN18,VMIPI, VEFUSE,VIO28, VIBR,VUSB33 and VBIF28	Iout= 0~0.8*Imax	1. Input power range 2. Typical capacitor 3. TA= -20°C ~+85°C	-5		+5	%
	Other LDOs			-2.5		+2.5	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax	1. Input power range 2. Typical capacitor 3. TA= -20°C ~+85°C	-5		+5	%
Load/Line regulation	Normal mode for ALDO, DLDO and SLDO	Iout= 0~Imax	1. Input power range 2. Typical capacitor 3. TA= 25°C	-1.5		+1.5	%
	VRTC and DVDD18_DIG	Iout= 0~0.3*Imax		-4		+4	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax		-4		+4	%
Power Off Voltage	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= -20°C ~+85°C 4. Iout= 0mA				0.1	V
Temperature coefficient	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= -20°C ~+85°C 4. Iout= 0 mA		-100		100	ppm/C
Load transient response	ALDO, DLDO and SLDO	Slew rate= 15mA/us	1. Input power range 2. Typical capacitor 3. TA= -20°C ~+85°C 4. Iout= 0.01*Imax~0.5*Imax	-5		+5	%
	VCN33, VA10, VSRAM_PROC, VDRAM, VLDO28, VGP3, VMC, VMCH, VEMC, VIO18	Slew rate= 0.5*Imax/us		-4		+4	%

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Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
Turn-on rise time	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA	20		300	us
Turn-on overshoot	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA			Vout*1.1	V
Power off Time	ALDO, DLDO and SLDO	Bypass capacitor ≦ 2.2uF; 1. Input power range 2. TA= +25°C 3. Iout= 0mA			4	ms
Power off Time	ALDO, DLDO and SLDO	Bypass capacitor ≦ 4.7uF; 1. Input power range 2. TA= +25°C 3. Iout= 0mA			8	ms
Power off Time	ALDO, DLDO and SLDO	Bypass capacitor ≦ 10uF; 1. Input power range 2. TA= +25°C 3. Iout= 0mA			12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout=0.2*Imax ~0.5*Imax		90		uVrms
Output noise	DLDO and SLDO	Freq = 10Hz to 80kHz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout=0.2*Imax ~0.5*Imax		500		uVrms
Output noise	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout=0.2*Imax ~0.5*Imax		1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0.2*Imax / 0.5*Imax		65		dB
PSRR	ALDO	Freq= 3kHz to 30kHz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0.2*Imax / 0.5*Imax		45		dB
PSRR	DLDO and SLDO	Freq = 217Hz; 1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0.2*Imax / 0.5*Imax		40		dB
Short current	VMCH and VEMC	OC; 1. Input power range 2. Typical capacitor 3. TA= +25°C	1.2 x Imax		3 x Imax	
Short current	VMCH and VEMC	OCFB; 1. Input power range 2. Typical capacitor 3. TA= +25°C	0.2 x Imax		1 .2x Imax	
Short current	ALDO, DLDO and SLDO	OC; 1. Input power range 2. Typical capacitor 3. TA= +25°C	1.2 x Imax		5 x Imax	
Short current	ALDO, DLDO and SLDO	OCFB; 1. Input power range 2. Typical capacitor 3. TA= +25°C	0.2 x Imax		1.2 x Imax	
Normal mode quiescent current	VCAMA, VSRAM_PROC, VDRAM, VMCH, VEMC and VCAMD	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			300	uA
Normal mode quiescent current	Other LDOs	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			55	uA
Normal mode quiescent current	VRTC and DVDD18_DIG	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			7	uA
Low power mode quiescent current	VSRAM_PROC, VMCH, VLDO28 and VEMC	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			15	uA
Low power mode quiescent current	Other LDOs	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			10	uA

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2.7 Driver

Table 2-7. Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
ISINK					
ISINK LED sink current	ISINK_SEL = 000		4		mA
	ISINK_SEL = 001		8		mA
	ISINK_SEL = 010		12		mA
	ISINK_SEL = 011		16		mA
	ISINK_SEL = 100		20		mA
	ISINK_SEL = 101		24		mA
ISINK dropout voltage	4 ~ 24mA VISINK drop		150	250	mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS
Pre-Charge Indicator					
LED sink current	VBAT=2.2V~4.5V Visink=1.5V~2.8V	1.6	2	2.4	mA
		3.2	4	4.8	mA
		4.8	6(default)	7.2	mA
Dropout voltage	VBAT=2.2V-4.5V 2mA~6mA Visink drop			1.5	V
Rise/Fall time	VBAT=3.4/3.8/4.2V Visink>1.5V			3.33	uS
Breath mode two step rising/falling time	Two step corner rate		30		%
VIBR					
Output voltage	VIBR_SEL = 000	1.1	1.2	1.3	V
	VIBR_SEL = 001	1.2	1.3	1.4	V
	VIBR_SEL = 010	1.4	1.5	1.6	V
	VIBR_SEL = 011	1.7	1.8	1.9	V
	VIBR_SEL = 100	2.35	2.5	2.65	V
	VIBR_SEL = 101	2.65	2.8	2.95	V
	VIBR_SEL = 110	2.85	3.0	3.15	V
	VIBR_SEL = 111	3.1	3.3	3.5	V
Output current			100		mA

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2.8 Audio CODEC

Table 2-8. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Headphone Output (Single-ended Output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +6dB, 24bit audio data					
P_{OUT}	Maximum output power @<0.1% THD		33.8		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		109		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -96 -97 -94		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -94 -95 -92		dB
NF_{OUT}	Output Noise Floor (A-weighted)		3.3		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)	16	32		Ω
C_{LOAD}	Output Capacitor Load			250	pF
$APGR_{DL}$	Analog Programmable Gain Range	-10		8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
XT_{LR}	L/R Channel Separation		-90		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_HPL/R)		90		dB
DAC to Headphone Output (Single-ended Output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +3dB, 24bit audio data					
P_{OUT}	Maximum output power @<0.1% THD		44		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		109		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -93 -97 -96		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -91 -95 -94		dB
NF_{OUT}	Output Noise Floor (A-weighted)		3.3		µVrms (A)

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

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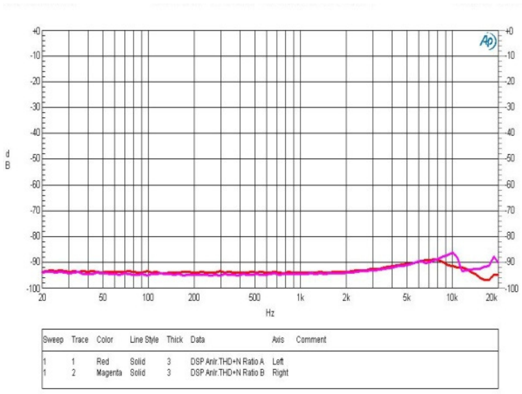
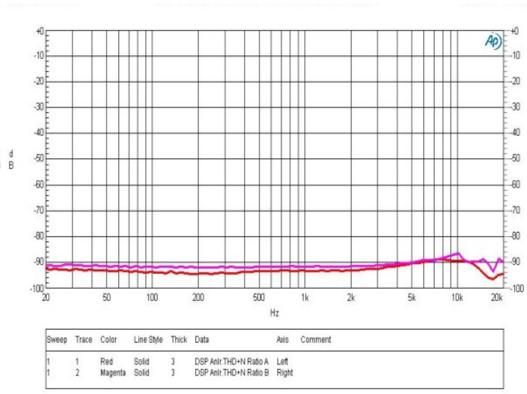
Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Headset Output (Differential Outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +3dB, 24bit audio data					
P_{OUT}	Maximum output power @<1% THD		136		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		-111		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -97 -99		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -95 -98		dB
NF_{OUT}	Output Noise Floor (A-weighted)		4.5		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)	16	32		Ω
C_{LOAD}	Output Capacitor Load			250	pF
$APGR_{DL}$	Analog Programmable Gain Range	-10		8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_HSP/N)		90		dB
DAC to Headset Output (Differential Outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +0dB, 24bit audio data					
P_{OUT}	Maximum output power @<1% THD		165		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		-107		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -97 -99		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -95 -98		dB
NF_{OUT}	Output Noise Floor (A-weighted)		4.5		µVrms (A)

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer



(a) P_{OUT}=10mW



(b) P_{OUT}=22.5mW

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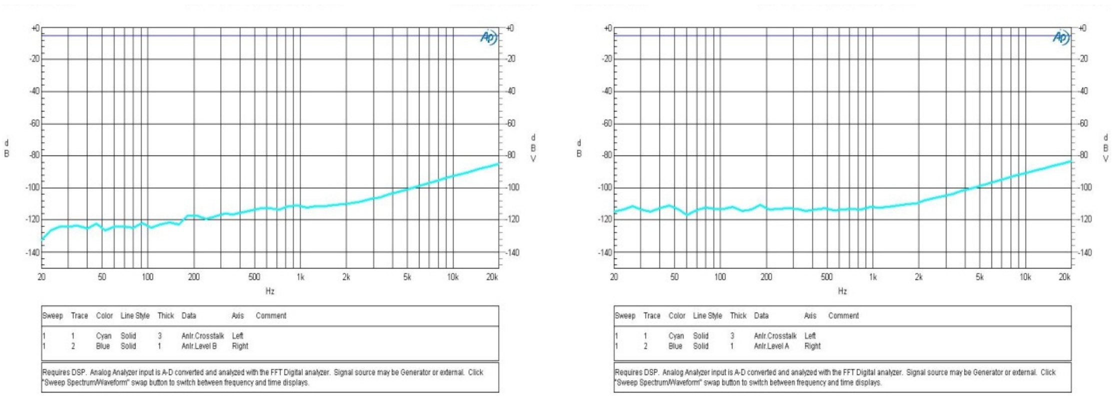
Figure 2-1. Audio Path THD+N v.s. frequency



(a)Xtalk RtoL **(b)Xtalk LtoR**

Figure 2-2. Audio path Xtalk v.s. frequency @P_{OUT}=10mW

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Line-out Output (Differential Outputs, AU_LOLP/N; R_{LOAD} = 600) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +3dB, 24bit audio data					
P_{OUT}	Maximum output power @<1% THD @PGA_{DL} gain =+3dB gain		60		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		-100		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 3.2mW		-110		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 3.2mW		-100		dB
NF_{OUT}	Output Noise Floor (A-weighted)		5		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)		600		Ω
C_{LOAD}	Output Capacitor Load			500	pF
$APGR_{DL}$	Analog Programmable Gain Range	-10		8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_HSP/N)		90		dB

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Table 2-9. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue Input Pahts to ADC (Differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to Noise Ratio		100		dB
N_{IN}	Input-referred Noise		14		µVrms
THD	Total Harmonic Distortion (THD) @0dBV(-3dBFS) input		-87		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
THD+N	THD Plus Noise (THD+N) @0dBV(-3dBFS) input		-86		dB
	THD Plus Noise (THD+N) @-60dBV(-63dBFS) input		-37		dB
Analogue Input Pahts to ADC (Differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to Noise Ratio		94		dB
N_{IN}	Input-referred Noise		3.6		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-84		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-31		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue Input Pahts to ADC (Differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to Noise Ratio		100		dB
N_{IN}	Input-referred Noise		14		μVrms
THD	Total Harmonic Distortion (THD) @0dBV(-3dBFS) input		-87		dB
THD+N	THD Plus Noise (THD+N) @0dBV(-3dBFS) input		-85		dB
	THD Plus Noise (THD+N) @-60dBV(-63dBFS) input		-37		dB
Analogue Input Pahts to ADC (Differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to Noise Ratio		94		dB
N_{IN}	Input-referred Noise		3.2		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-85		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-32		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD30_AUD, AVSS30_AUD], and the suggested maximum input swing Vpp ≤ 1Vrms (0 dBV) @ PGA_{UL} gain = 0dB

General

Symbol	Parameter	Min.	Typ.	Max.	Unit
$APGR_{UL}$	Uplink Analog Programmable Gain Range	0		24	dB
$APGS_{UL}$	Uplink Analog Programmable Gain Step		6		dB
CMRR	Common-mode Rejection Ratio @-18dBV, 1KHz sinusoid signal to both pins of an input configured differentially	40	72		dB
XT_{TALK}	ULL-to-ULR Channel Separation @ one input terminated with -18dBV, 1KHz sinusoid signal. Measure digital output of terminated channel	60	100		dB
XT_{DL2UL}	DL-to-UL Channel Separation @ 0dBV, 1KHz Rx path with RLOAD = 32	60	105		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		70		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		70		dB
	10kHz @ 200 mVpp square wave imposed on power.		70		dB

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General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
	Measure digital output				
$F_{S,UL}$	Audio Uplink Sampling Rate 8, 16, 32, 48, 96, and 192 KHz	8		192	KHz

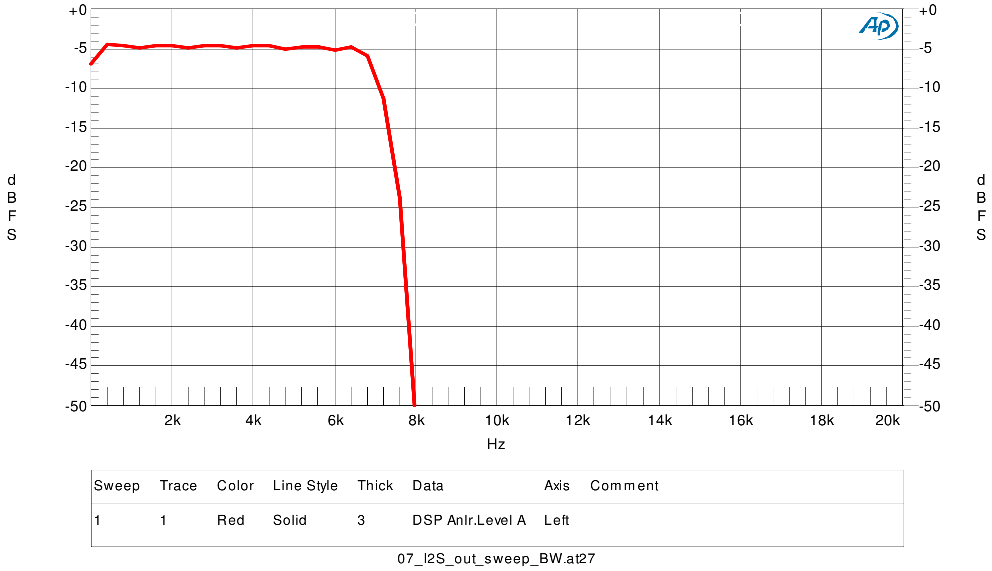

Figure 2-3. Frequency response (16kHz)

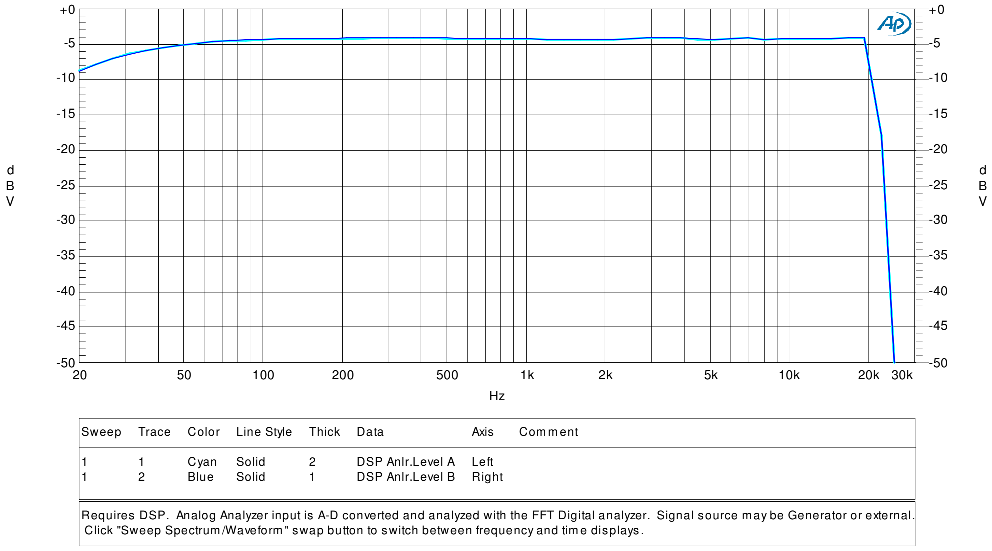

Figure 2-4. Frequency response (48kHz)

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Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency	0.514	3.25/ 1.62	4.33	MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

Table 2-10. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1µF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone Bias Voltage	1.7		2.7	V
V_{OUT} Step	Bias Voltage Output Step Size 1.7~2.1 2.5~2.7		0.1		V
I_{OUT}	Maximum Output Current (Two MICBIAS loads total)			3	mA
N_{OUT}	Output Integrated Noise (20~20kHz A-weighted) with 1µF cap.		4.7		µVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		2.8		dB
PSRR	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
PSRR	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
$C_{LOAD,MIC}$	Output Capacitor Load on MICBIAS		96		µF

Table 2-11. ACCDET specifications

Accessory Detection (ACCDET1)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1& 1.5kΩ (1%) MICBIAS resistors *2: The characteristics assume no other component is connected to ACCDET. *3: The key detection voltage will be normalized automatically. For different micbias settings , the same key (resistance is the same) is pressed, and the read voltage (key pressed) value will be similar.				
-	4-pole Microphone Detection	2K		14K	Ω
-	Microphone impedance detection after 4-pole microphone plugged-in				
-	MICD_LVL[0]: Down key	400		620	Ω
-	MICD_LVL[1]: Up key	150		320	Ω
	MICD_LVL[2]: Hook key	0		100	Ω
Accessory Detection (ACCDET2)					
-	5 pole (2nd) Microphone Detection	2K		14K	Ω

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2.9 Battery Charger

Table 2-12. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN operating voltage		4	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT CHRIN detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4		10.5	V
HV adaptive current @ pre_charge	CHRIN rising switch threshold (300mA => 70mA)		7		V
	CHRIN falling switch threshold (70mA => 300mA)		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-50		+50	mV
VBAT CV voltage accuracy	Programmable: 3.5~4.6 V	-30		+30	mV
VBAT OV voltage accuracy	Programmable: 3.8~4.7 V	-30		+30	mV
CC mode charging current accuracy	Programmable:450 ~2000 mA (Rsense=56mΩ)	10		10	%
	Programmable:200 mA/300 mA (Rsense=56mΩ)	20		20	%

2.10 BC1.x

Table 2-13. BC1.x specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port	35	70	94	mA
	Standard charging down-stream port	35	70	94	mA
	DP, DM short	210	300	390	mA
BC11 characteristics	DP, DM floating	210	300	390	mA
	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min

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2.11 Down Load Without Battery

Table 2-14. Download without batteryspecifications

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

2.12 AUXADC

Table 2-15. AUXADC specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Supply voltage		1.7	1.8	1.9	V
Resolution	AUXADC_VIN			15	Bits
	Others			12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1		+1	%
Gain error	Relative to full-scale	-1		+1	%
INL	15-bit output	-2		+2	LSB
DNL	15-bit output	-2		+2	LSB
Current consumption			350		uA

2.13 Fuel Gauge

Table 2-16. Fuel gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/16		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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2.14 DCXO

Table 2-17. XO specification

Parameter	Test condition	Title	Unit	Min.	Typ.	Max.
Supply current in suspend (OSC LPM)	VXO22=2.2V; without 32K RTC	$I_{xo,lpm}$	uA		50	
Supply current in idle (OSC + one buffer for SOC)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,idle}$	mA		2	
Supply current in RF TRx (OSC + buffers for SOC, RF_Cell)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,trx}$	mA		4	
Extra Supply current for RF_Conn	VXO22=2.2V; PCB Cload<20pF	$I_{xo,conn}$	mA		2	
Extra Supply current for RF_NFC	VXO22=2.2V; PCB Cload<20pF	$I_{xo,nfc}$	mA		1	
Leakage current	VXO22=2.2V; with 32K RTC	$I_{xo,leak}$	uA			1
Center operating frequency	Internal resonant; with QVL crystal	F_{dcxo}	MHz		26	
Duty cycle	Square wave in high driving mode		%	45	50	55
Static tuning range	XTAL1/2 differential input capacitance	C_{TR}	pF	4.0		8.5
CapID binary bits	CDAC		bit		8	
Startup time, after clock request	Delta f < 1ppm.	$T_{startup}$	ms		1	2
Crystal input pins	Specific foundries		pin		2	
Crystal size	CL=7~7.5pF				2520	3225

Table 2-18. Reference input buffer specification (XTAL1, buffer mode)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	3	5		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		5	10	pF

This pin should be AC coupled when used with an external clock source.

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3 Functional Descriptions

3.1 General Descriptions

MT6351 is a fully integrated PMIC target for smart phone power provider. Figure 3-1. is the block diagram of MT6351 PMIC.

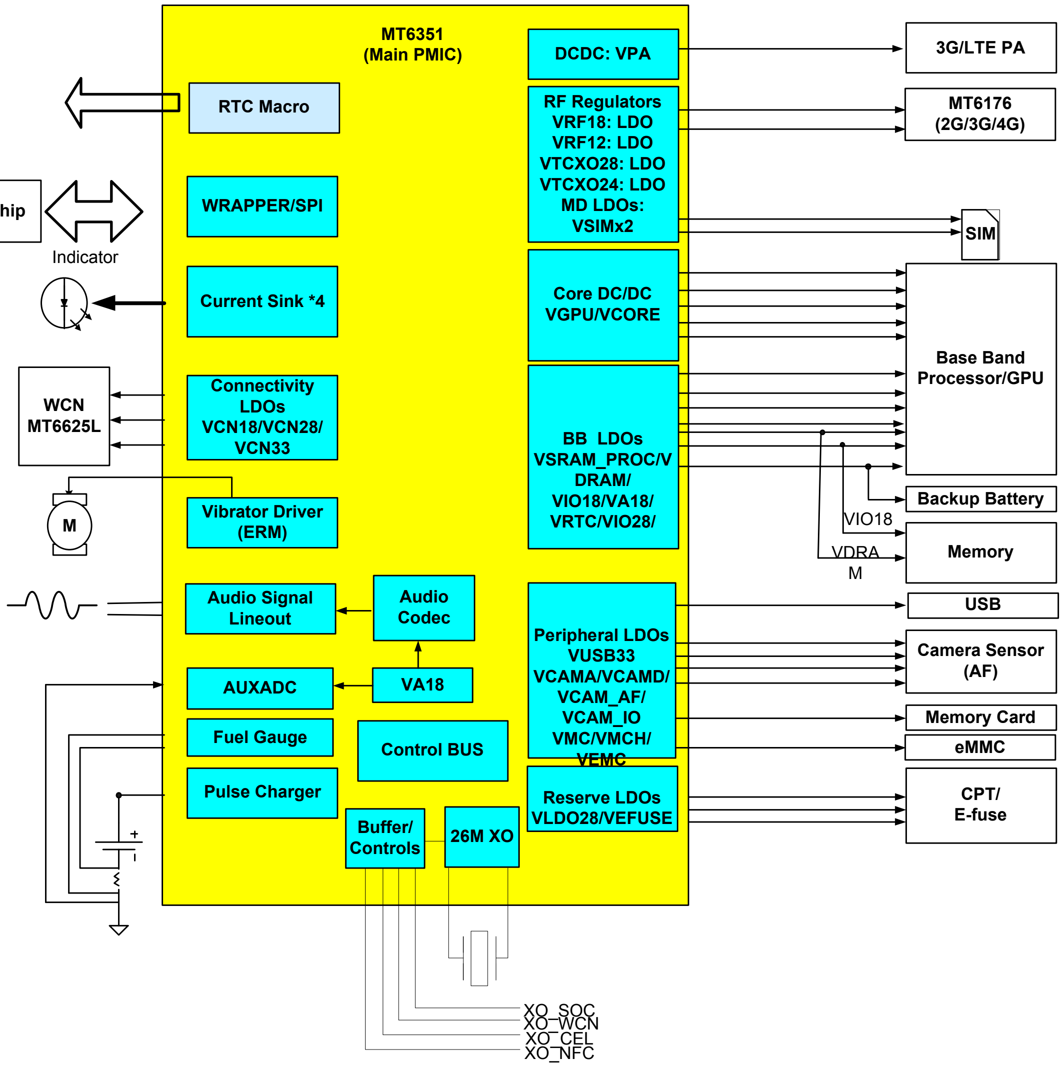

Figure 3-1. MT6351 block diagram

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3.2 PMIC Functional Blocks

MT6351 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6351 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator
- Vibrator driver: Provides regulated power for vibrator.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ UVLO_VTHH) nor in the thermal condition, there are 3 methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Setting BBWAKEUP to high
3) Valid charger plug-in

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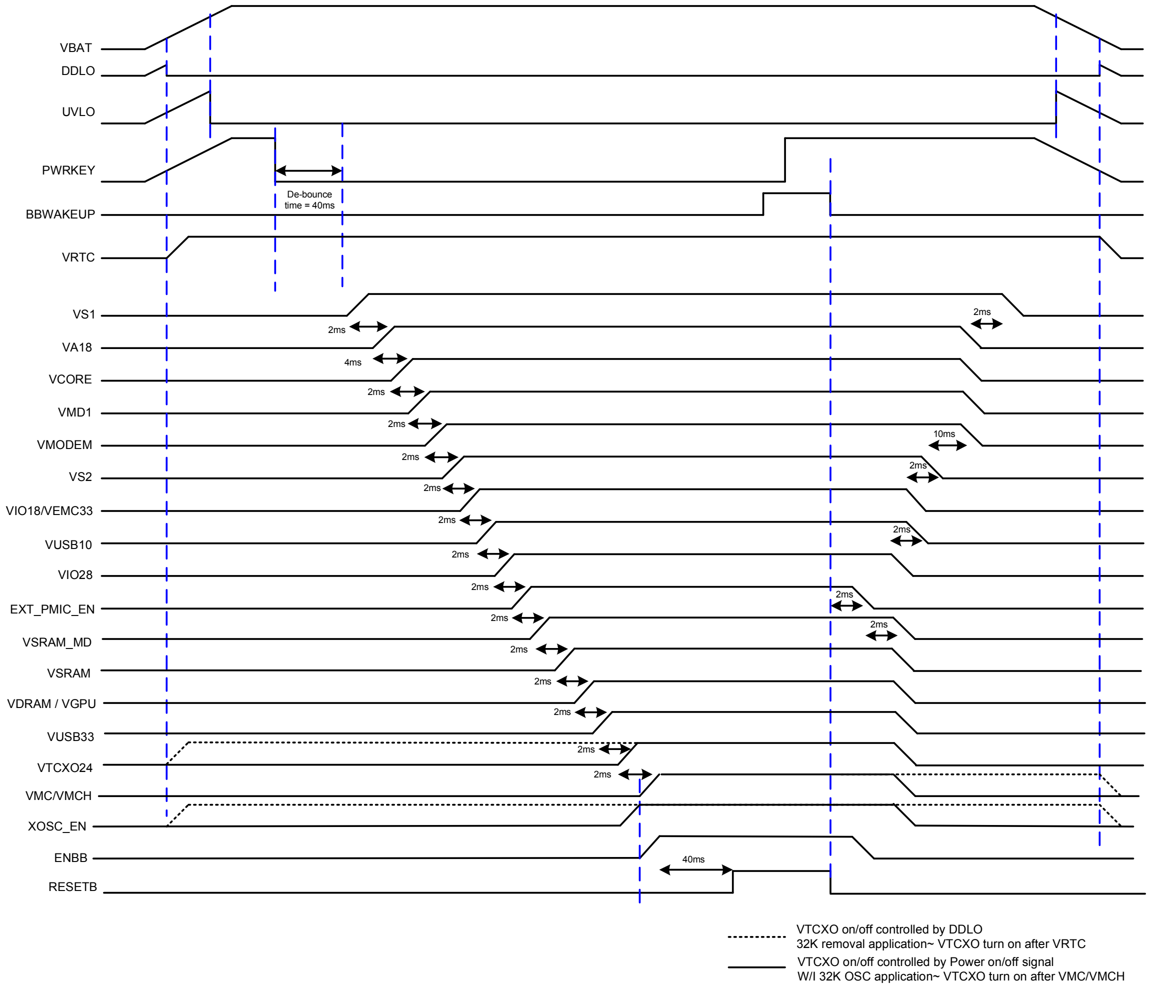

Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

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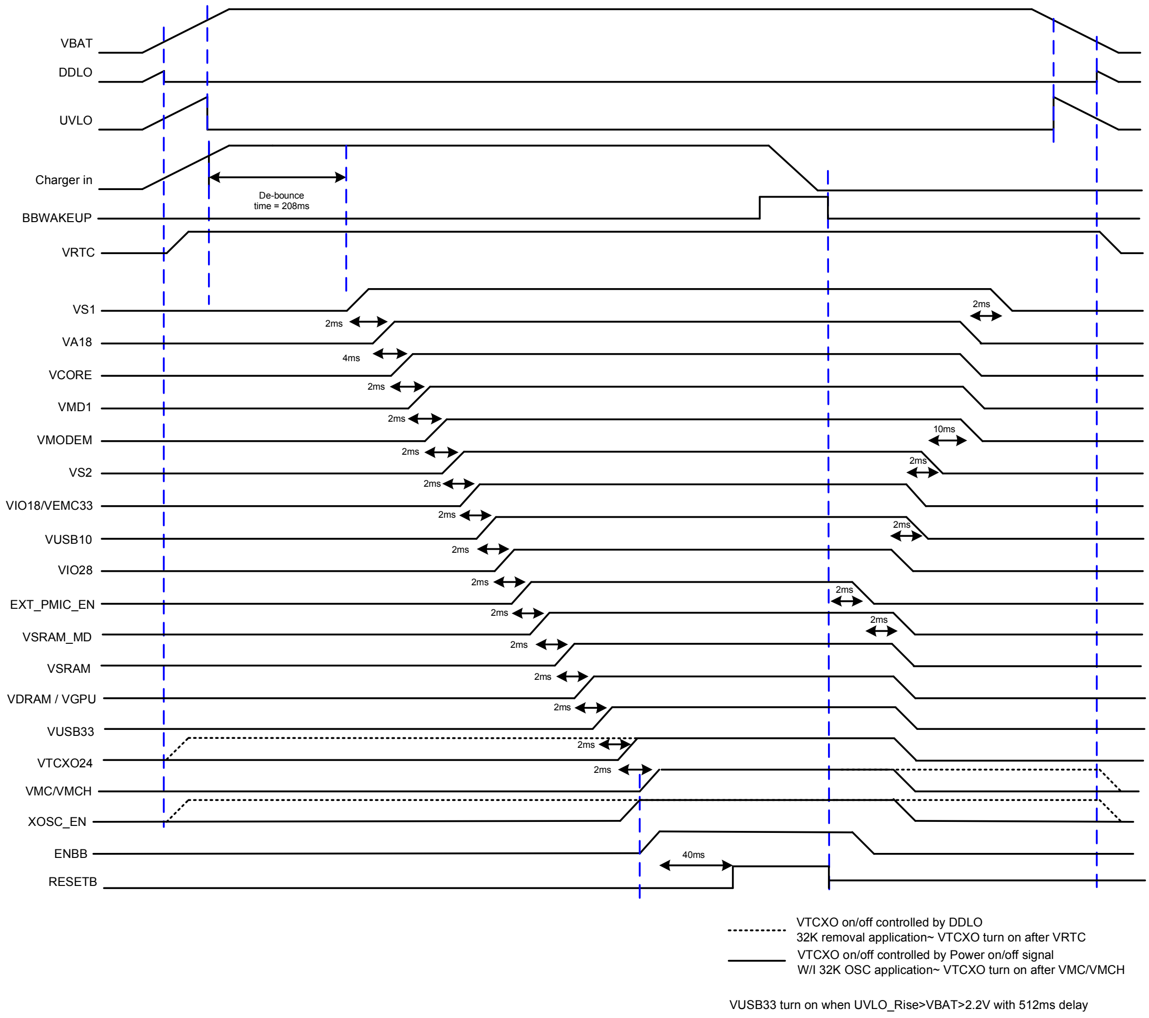

Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2. RTC module generates BBWAKEUP to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage> CHGIN_VTHH and VSYS>UVLO, the handset will also be powered on.

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Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSNS (with charger plugged in) and VBATSNS+VSYSNS (without charger plugged in). It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are 8 buck converters in MT6351 to efficiently generate regulated power for graphic processor, digital core and circuits. The block diagram is shown in Figure 3-1. The buck converters operate with 3 or 2MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

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Table 3-1. Buck converter brief specifications (MT6351V for MT6755/6797 series)

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VCORE	1	0.6 ~ 1.31	6.25	3,000	Y	Digital core always on domain (CORE_AO) ※for 3A Imax Output Current: (1) Input Voltage > 3.1 (2)TA<55℃
VGPU	1	0.6~1.31	6.25	3,000	Y	GPU ※for 3A Imax Output Current: (1) Input Voltage > 3.1 (2)TA<55℃
VSRAM_MD	1	0.6 ~ 1.31	6.25	1,200	Y	SRAM for MODEM
VMODEM	0.9	0.6 ~ 1.31	6.25	1,200	Y	MODEM
VMD1	0.9	0.6 ~ 1.31	6.25	1,200	Y	MODEM
VS2	1.35	1.35 ~ 1.5	50	2,000	Y	SYS LDOs power
VS1	2	2	50	2,000	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	800	N	3G/LTE PA

Table 3-2 Buck converter brief specifications (MT6351DV for MT6757 series)

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VCORE	0.8	0.6 ~ 1.31	6.25	3,000	Y	Digital core always on domain (CORE_AO) ※for 3A Imax Output Current: (1) Input Voltage > 3.1 (2)TA<55℃
VGPU	0.8	0.6~1.31	6.25	3,000	Y	GPU ※for 3A Imax Output Current: (1) Input Voltage > 3.1 (2)TA<55℃
VSRAM_MD	0.9	0.6 ~ 1.31	6.25	1,200	Y	SRAM for MODEM
VMODEM	0.8	0.6 ~ 1.31	6.25	1,200	Y	MODEM
VMD1	0.7	0.6 ~ 1.31	6.25	1,200	Y	MODEM
VS2	1.35	1.35 ~ 1.5	50	2,000	Y	SYS LDOs power
VS1	2	2	50	2,000	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	800	N	3G/LTE PA

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-3. LDO types and brief specifications

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VTCXO28	VBAT_LDOS1	2.8	2.8	40mA	N	RFFE

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VTCXO24	VSYSSNS	2.375	2.375	40mA	Y	DCXO
ALDO	VXO22	VSYSSNS	2.2	2.2	40mA	Y	DCXO
SLDO	VRF18	AVDD20_SLDO1	1.81	1.81	400mA	N	RF
SLDO	VRF12	AVDD14_SLDO2	1.2	1.2	145mA	N	RF
DLDO	VCN33	VBAT_LDOS4	3.3	3.3/3.4/ 3.5/3.6	500mA	N	WCN
ALDO	VCN28	VBAT_LDOS1	2.8	2.8	40mA	N	WCN
SLDO	VCN18	AVDD20_SLDO1	1.8	1.8	200mA	N	WCN
ALDO	VCAMA	VBAT_LDOS1	2.8	2.8	300mA	N	CAMERA
SLDO	VCAMIO	AVDD20_SLDO1	1.8	1.8	200mA	N	CAMERA
SLDO	VCAMD	AVDD14_SLDO2	1.21	0.9/1.0/1.05 /1.1/1.21	1,200mA	N	CAMERA
SLDO	VA10	AVDD14_SLDO2	0.9	0.9/0.95 /1.0	300mA	Y	USB3.0
ALDO	VA18	VBAT_LDOS3	1.8	1.8	40mA	Y	Audio
SLDO	VSRAM_PROC	AVDD14_SLDO3	1.1 (MT6351V) 1.025 (MT6351DV)	0.6~1.2	250mA	Y	SRAM
SLDO	VDRAM	AVDD14_SLDO1	1.21	1.21	1,200mA	Y	DRAM
DLDO	VSIM1	VBAT_LDOS3	1.8	1.7/1.8/ 1.86/2.76/ 3.0/3.1	100mA	N	SIM#1 card
DLDO	VSIM2	VBAT_LDOS3	1.8	1.7/1.8/ 1.86/2.76/ 3.0/3.1	100mA	N	SIM#2 card
SLDO	VMIPI	AVDD20_SLDO1	1.8	1.8	200mA	N	MIPI
DLDO	VLDO28	VBAT_LDOS4	2.8	2.8	800mA	N	Touch Panel and CAMERA _AF
SLDO	VGP3	AVDD20_SLDO2	1.81	1.0/1.05/1.1 /1.22/1.3/ 1.5/1.8/1.81	300mA	N	General purpose

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
DLDO	VEFUSE	VBAT_LDOS3	1.8	1.71/1.8/ 1.89/2.0/ 2.1/2.2V	200mA	N	EFUSE
DLDO	VIO28	VBAT_LDOS3	2.8	2.8	200mA	Y	IO and Sensor
DLDO	VMC	VBAT_LDOS2	2.9	1.8/2.9/ 3.0/3.3	200mA	Y	MSDC
DLDO	VMCH	VBAT_LDOS3	2.9	2.9/3.0/3.3	800mA	Y	SD Card
DLDO	VEMC	VBAT_LDOS4	2.9	2.9/3.0/3.3	800mA	Y	EMMC and UFS
DLDO	VIBR	VBAT_LDOS2	2.8	1.2/1.3/1.5/ 1.8/2.0/2.8/ 3.0/3.3	200mA	N	Vibrator
ALDO	VUSB33	VBAT_LDOS4	3.07	3.07	100mA	Y	USB1.0
ALDO	VBIF28	VBAT_LDOS1	2.8	2.8	20mA	N	BATTERY MIPI
SLDO	VIO18	AVDD20_SLDO2	1.8	1.8	1,000mA	Y	IO and EMMC5.0
VRTC	VRTC	VSYSSNS	2.8	2.8	2mA	Y	RTC macro
VDIG18	DVDD18_DIG	VSYSSNS	1.8	1.8	20mA	Y	PMIC digital

3.2.4 Drivers

MT6351 supports 4 indicator LED drivers at most. The following figure depicts the major application for indicator LEDs drivers. LED driver of MT6351 supports PWM mode and Breath mode.

The LED current is from small to large then descends; this is the breath mode.

Through software programming the registers in Figure 3-5, MT6351 can change the breathing cycle time include Trising_1, Trising_2, Ton, Toff, Tfalling_1 and Tfalling_2 period.

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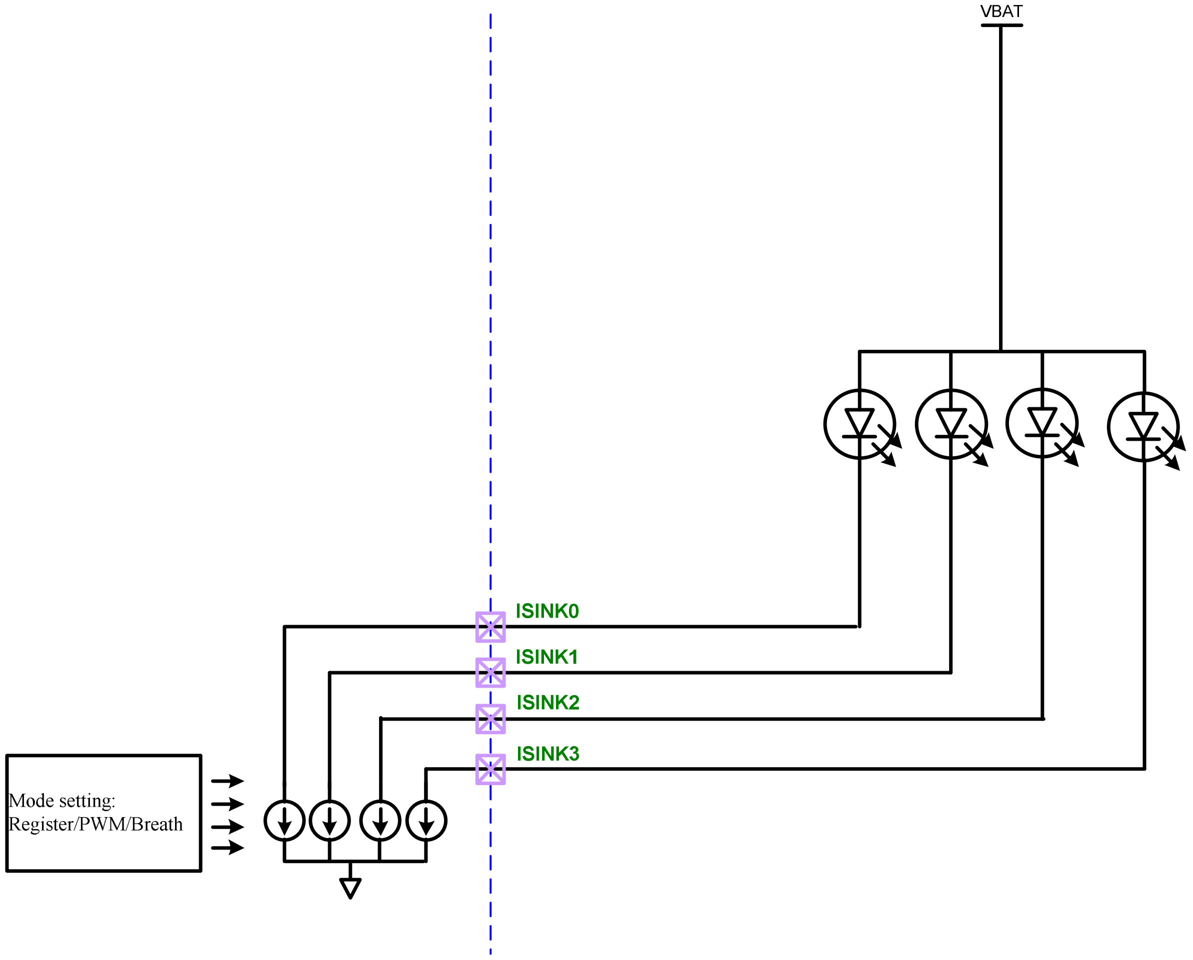

Figure 3-4. Configuration for indicator LED drivers

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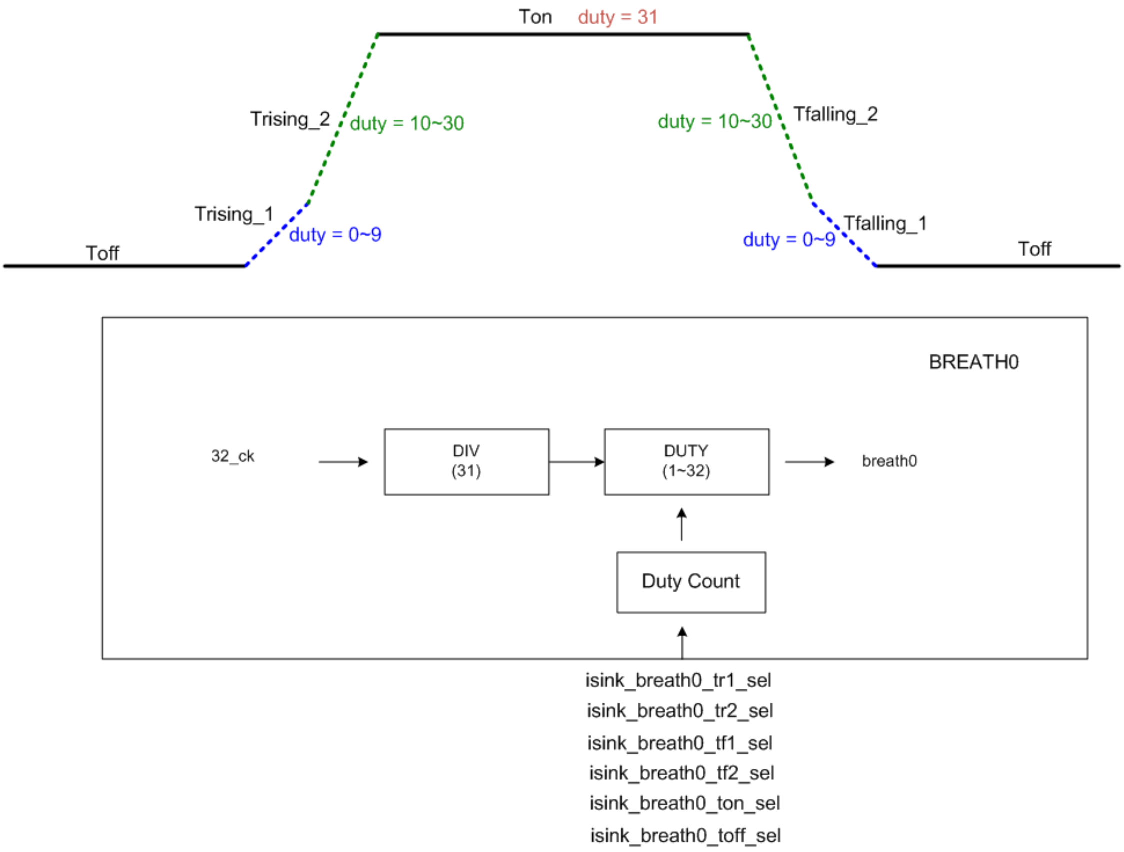

Figure 3-5. LED drivers breath mode

3.2.5 Pre-charge Indicator

MT6351 supports an indepentdent indicator LED driver (pre-charge indicator). Once the charger is plugged in, the indicator will turn on to indicate the system is being charged. It provides 2/4/6mA driving current. After the SW works, it will have the same function as other LED drivers do.

3.2.6 Vibrator Driver

The VIBR driver power allows up to 100mA current for ERM (Eccentric Rotating Mass) or coin type vibrator with programmable output voltage.

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3.2.7 Audio CODEC and Accessory Detection

3.2.7.1 Block Descriptions

The block diagram of audio codec is illustrated below. Audio uplink path is composed of PGA and audio ADC. There are four input pairs of the uplink path to support dual-MIC, earphone-MIC, ANC-MIC, and digital-MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers, a mono voice driver and a mono line-out driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The line-out drvier can be used to drive external high output power loud-speaker amplifier. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.

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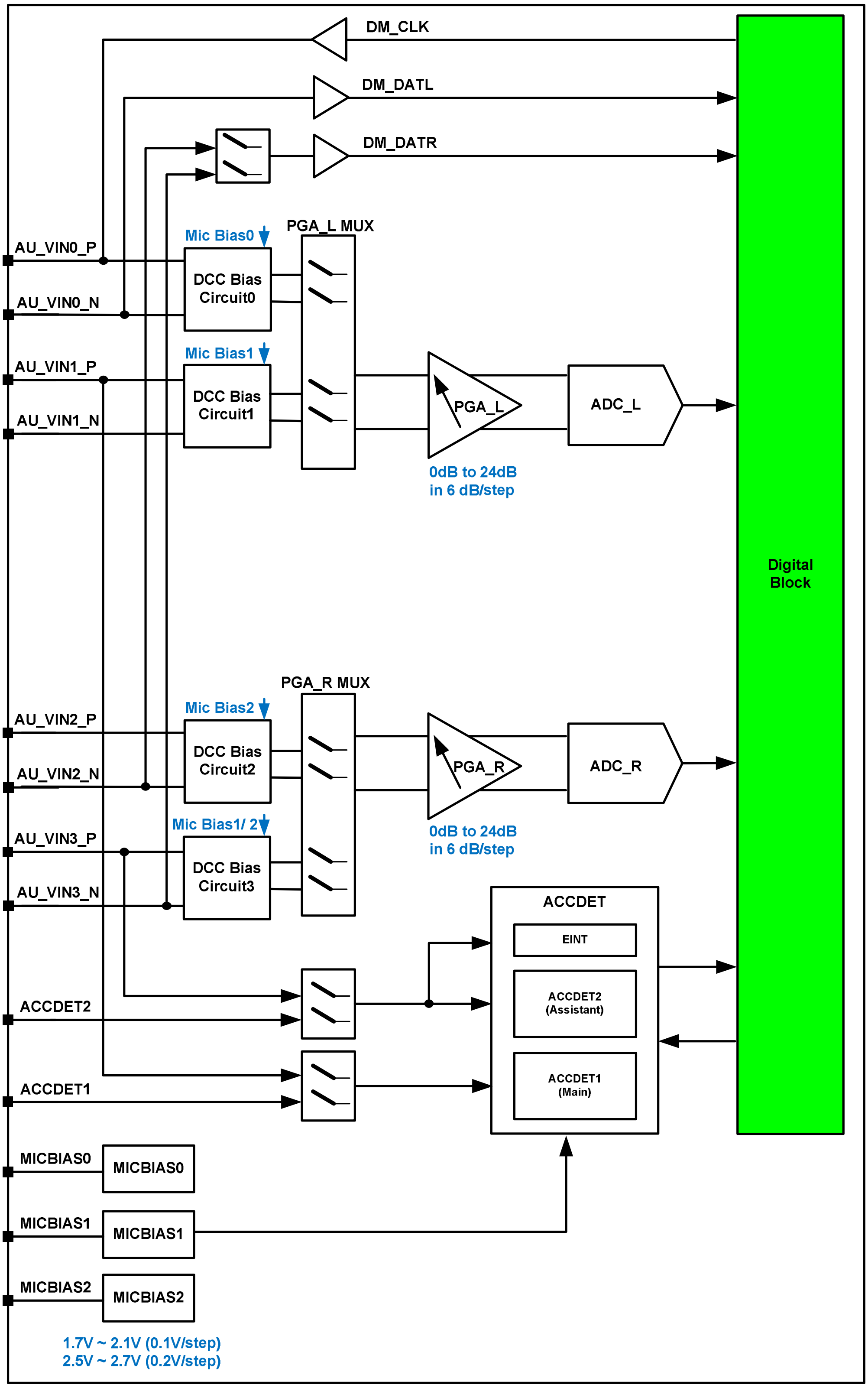

(a) Audio/speech uplink and accessory detection

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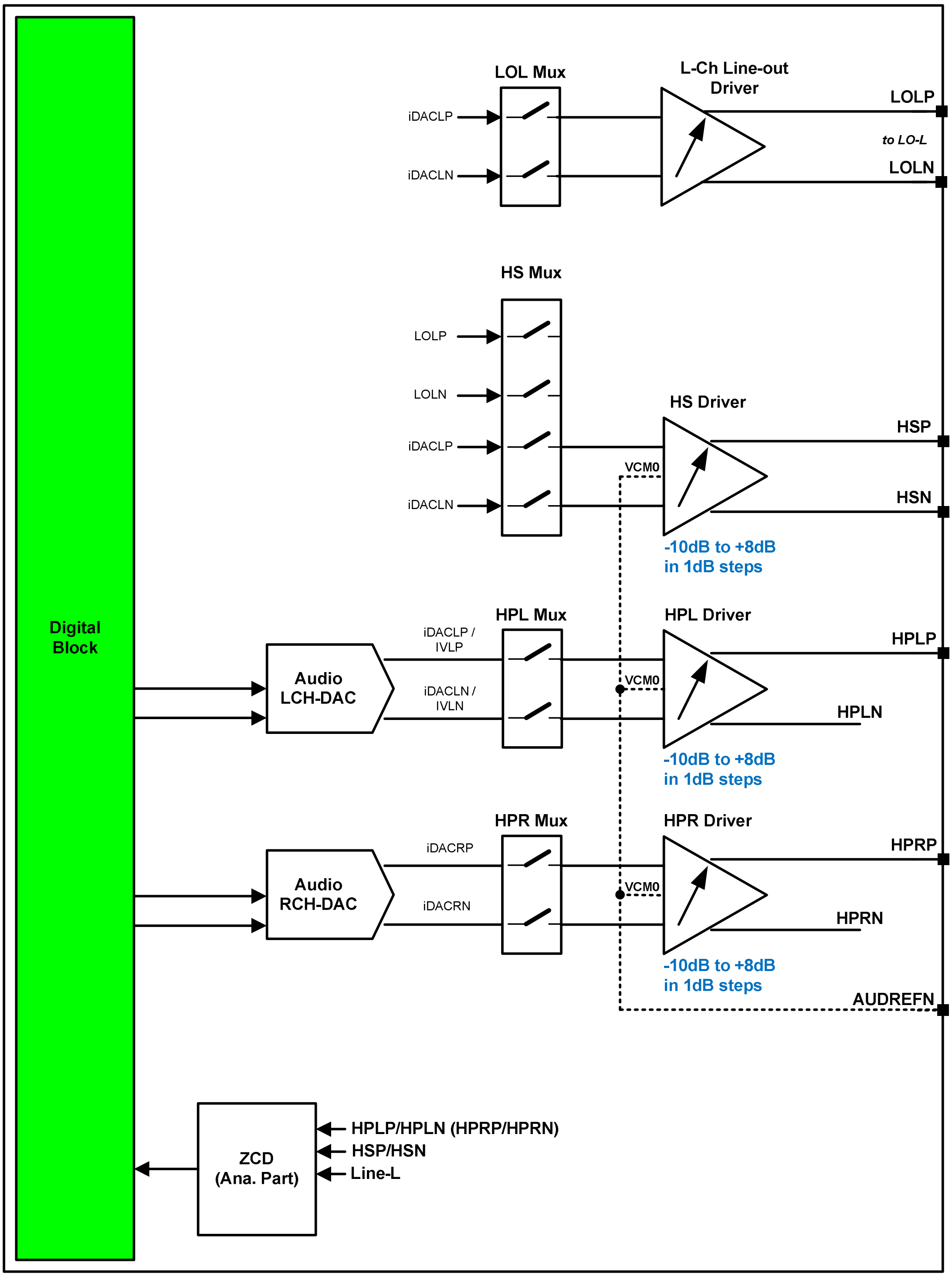

(b) Audio/speech downlink and headphone detection

Figure 3-6. Audio CODEC block diagram

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3.2.8 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

3.2.8.1 Block Descriptions

The block diagram of battery charger is illustrated below.

Charger block diagram

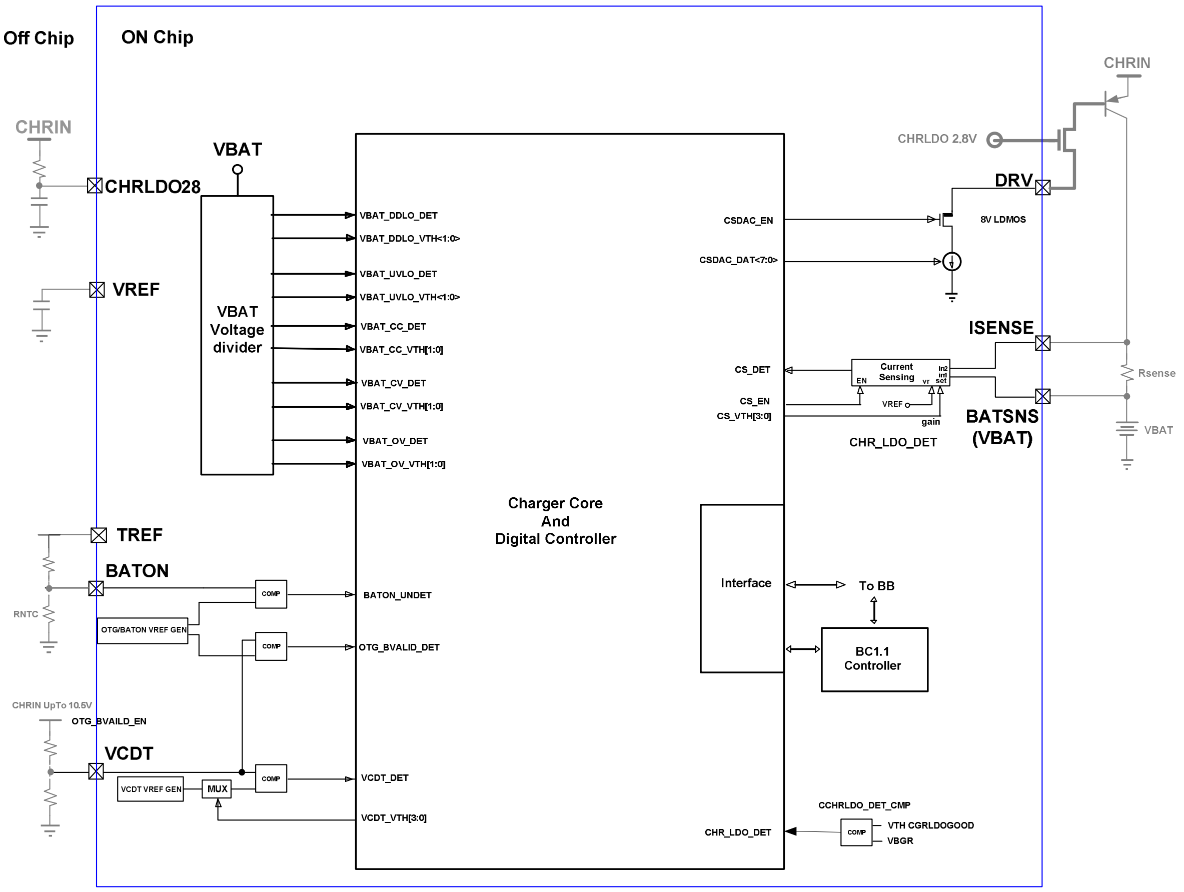

Figure 3-7. Block diagram of battery charger

3.2.8.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V, software default setting), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

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3.2.8.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.0V, PMIC power-off state), CC mode (Constant Current mode or fast charging mode at the range of 3.0V < VBAT < 4.2V, CV default voltage) and CV mode (Constant Voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

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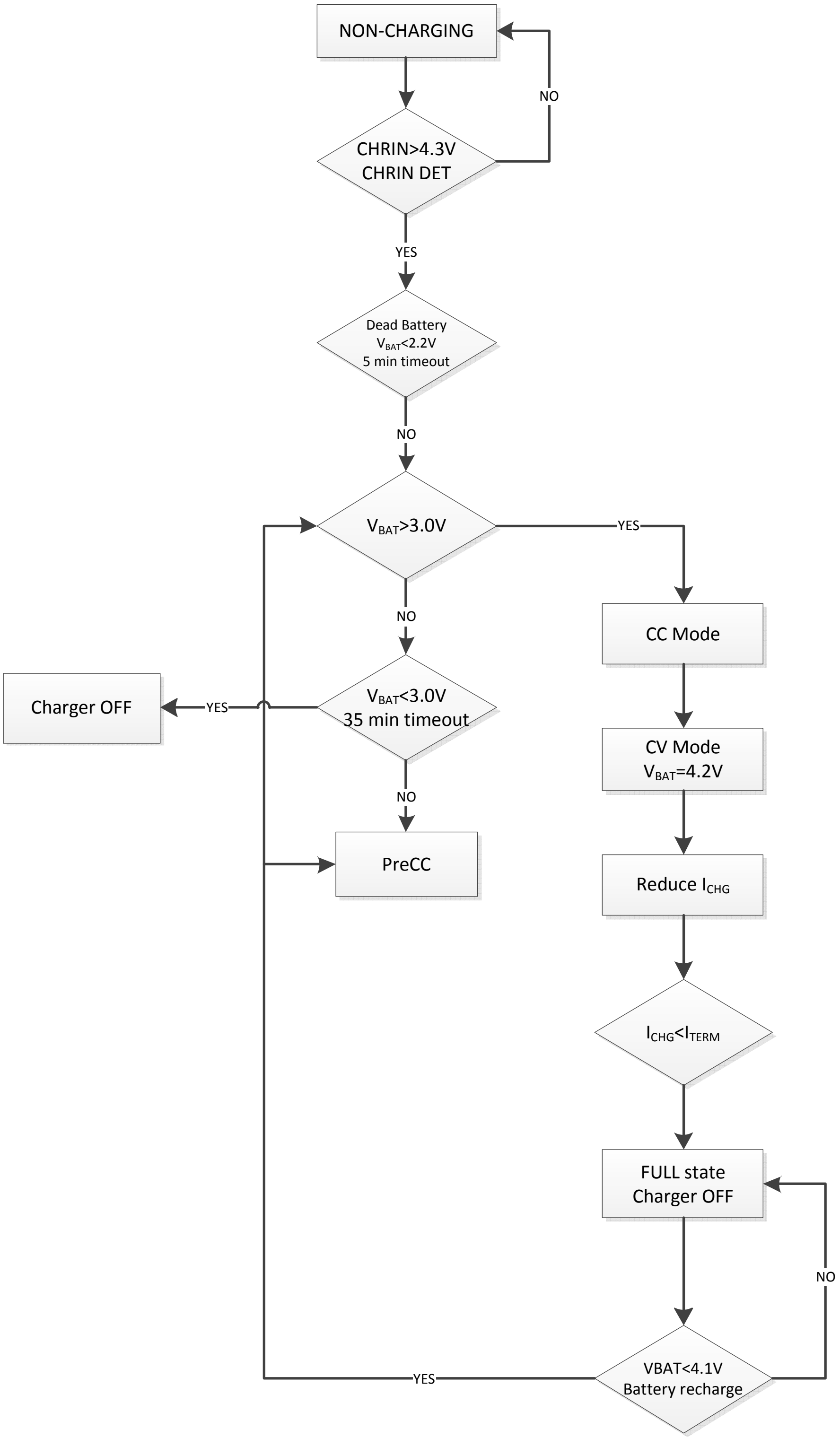

Figure 3-8. Flow chart of charging states

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external R_{SENSE} is kept around 16.8mV (AC charger) or 3.92mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,AC\,adapter} = \frac{V_{SENSE}}{Rsense} = \frac{16.8mV}{Rsense}$$

$$I_{PRECC1,USB\,HOST} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.0V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external R_{SENSE} resistor. The charging current can be determined by CS_VTH/ R_{SENSE}, where CS_VTH is programmed by registers. For example, if R_{SENSE} is selected as 0.056Ω, the CC mode charging current can be set from 70 to 2,000mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant-voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current gradually decreased step-by-step, and the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches termination current automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection will be activated and turns off the charger immediately.

3.2.8.1.3 BC1.x Dead-Battery Support

MT6351 also supports dead-battery condition BC1.x. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after the trickle current is applied, the charger will be disabled. On the other hand, once the battery voltage rises to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

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When the battery is below 3.0V, the charger will charge the battery by the PRECC1 current.
A dedicated 5 min. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.4V under charging. Another 35 min. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.0V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.8.1.4 Auto Power-On Mode (USB Download without Battery)

MT6351 features a default auto power-on mode (or USB DL without battery) no matter with or without battery. You can disable auto power-on by adding external pull-high resistor on the FCHR_ENB pin. You can still initiate USB DL (auto power-on) by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BAT_ON information can be detected through battery's NTC when it is connected to pin BAT_ON of MT6351.

3.2.9 AUXADC

3.2.9.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

Table 3-4. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.8
1	ISENSE	2.5 ~ 4.8
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 2.7
5	ACCDET	0 ~ 1.8
7	AUXADC_VIN	0 ~ 1.8
Others	Internal use	N/A

3.2.10 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn

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from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

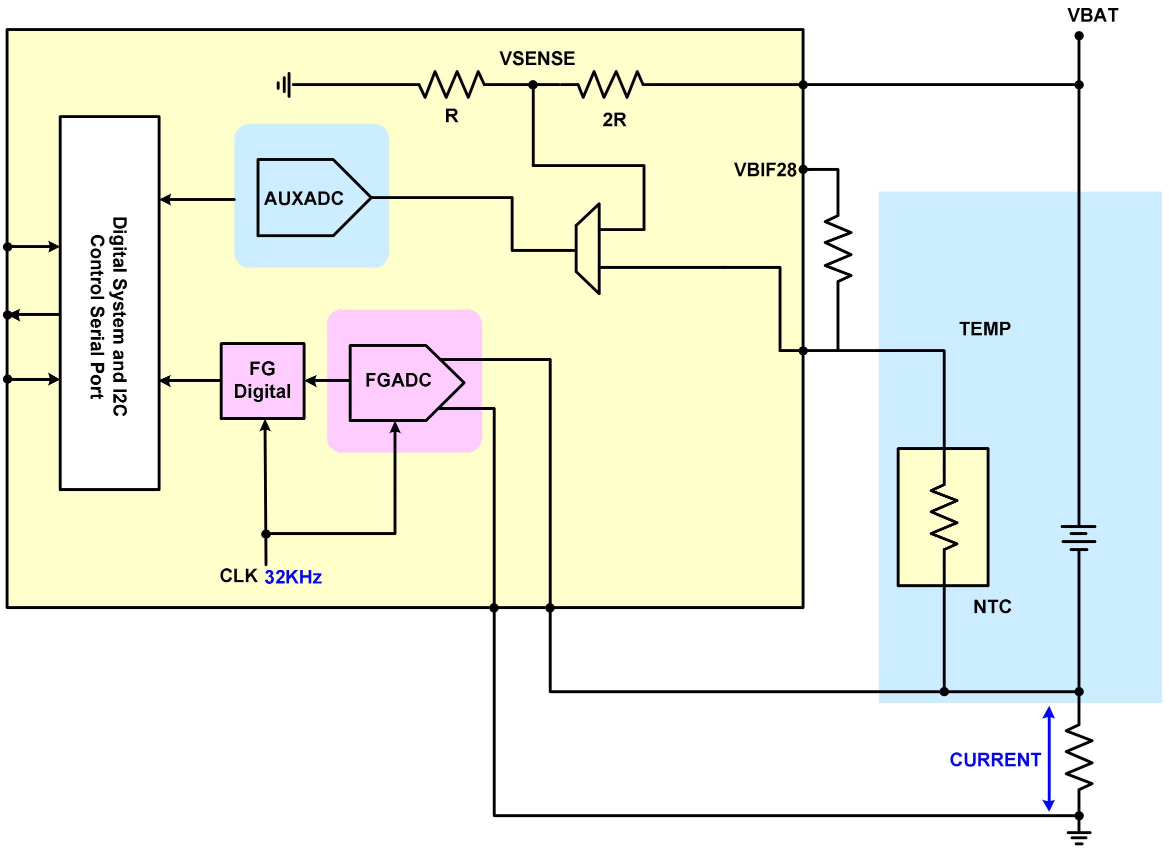

Figure 3-9. Fuel gauge block diagram and external connection

3.2.11 Real-Time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an

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alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6351, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. When crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

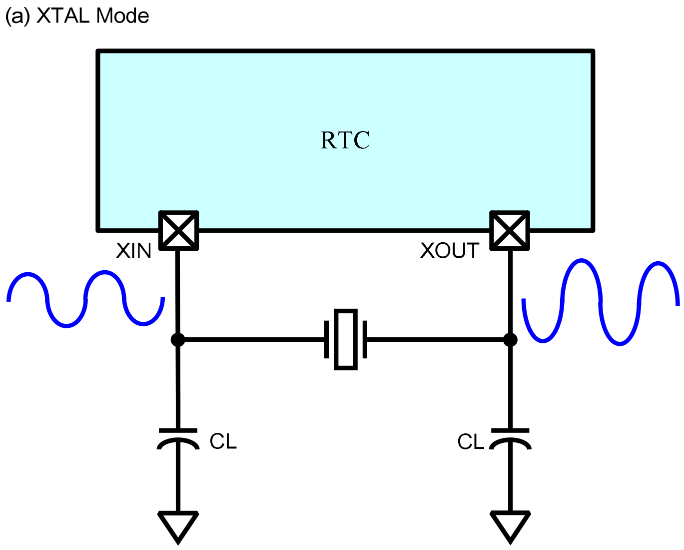

Figure 3-10. RTC configuration methods for XTAL

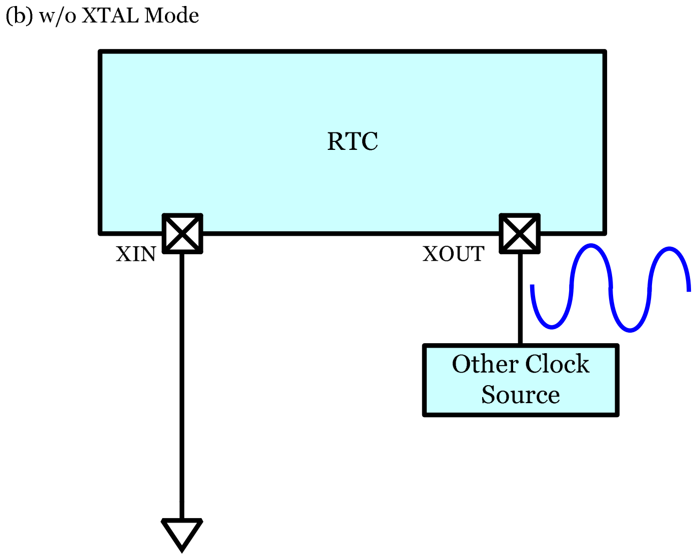

Figure 3-11. RTC configuration methods for w/o XTAL mode

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3.2.11.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

Table 3-5. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-20		80	°C

The minimum VRTC value means if the crystal oscillator starts up successfully, then the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, below are a few recommendations for the crystal parameters to be used well with XOSC32 in MT6351.

Table 3-6. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
Co	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than 3 times. If CL is selected larger, the frequency accuracy will be decreased, and the –R will degrade too.

3.2.12 DCXO

3.2.12.1 Reference Clock Specification

MT6351 PMIC integrates a core 26MHz XTAL oscillator (XO) and supports 32kHz RTC-removal low power mode. It also provides backward compatible (BCM) configurations for previous solutions.

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There are two High Performance (1.8V_{PP}) and two Low Power (1.1V_{PP}) external clock buffers for the entire system and one internal buffer for Audio.

The modes of operation are configured by two input pins, DCXO32K_EN and XMODE, and the definitions are shown as below.

DCXO32K_EN	XMODE	Mode
LOW	LOW	Buffer mode with external TCXO
LOW	HIGH	Oscillator mode with 32K RTC
HIGH	LOW	BC M mode, system clock from RF
HIGH	HIGH	Oscillator mode without 32K RTC

In oscillator mode, the Temperature Sensing Crystal (TSX) is connected between XTAL1 and XTAL2. In buffer mode, the external clock inputs from XTAL1. Keep XTAL2 pin NC.

Note that the logic of DCXO32K_EN and XMODE must be directly shorted to GND or VRTC28 so that MT6351 can select proper power-on-sequence for different system configurations.

3.2.12.2 Reference Output Buffer(s) Specification

There are four 26MHz clock output buffers driving out from the chip. They can be used as reference clocks for other chips and applications. Two High Performance (HP) external buffers output 0~1.8V squarer wave, and two Low Power (LP) external buffers output 0~1.1V squarer wave. Note that all their DC common mode voltage is not zero, so DC block capacitor is required if it is AC coupled and specific common mode voltage.

The current of all buffers can be optimized for different PCB Cloading. Typical current consumption is optimized for < 20pF Cloading.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty cycle		40		60	%
Rise/Fall time	10% to 90% of signal swing @ Cload=30pF			5	ns
HP buffer output	Square wave		1.8		Vp-p
HP SSB phase noise	1Hz offset [30pF load]			-50	dBc/Hz
	5Hz offset [30pF load]			-73	dBc/Hz
	10Hz offset [30pF load]			-80	dBc/Hz
	100Hz offset [30pF load]			-106	dBc/Hz
	1kHz offset [30pF load]			-134	dBc/Hz
	10kHz offset [30pF load]			-144	dBc/Hz

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Parameter	Conditions	Min.	Nom.	Max.	Unit
	100KHz offset [30pF load]			-152	dBc/Hz
HP current consumption	Zload = 20pF (each buffer)		2.0		mA
LP buffer output	Square wave		1.1		Vp-p
LP SSB phase noise	100Hz offset [30pF load]			-85	dBc/Hz
	1kHz offset [30pF load]			-110	dBc/Hz
	10kHz offset [30pF load]			-130	dBc/Hz
	100kHz offset [30pF load]			-130	dBc/Hz
LP current consumption	Zload = 20pF (each buffer)		1.0		mA

3.2.12.3 32kHz RTC Removal Mode

In low power mode a 32kHz clock is produced by a fractional-N divider (1st order Sigma Delta Modulated) to replace the traditional 32kHz XTAL. The capacitance is minimized for significant current reduced.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Frequency	Averaged value		32768		Hz
XO LPM current consumption	Low power mode With all capacitors switched off and auto-amplitude calibration on		50		µA
Duty cycle				70	%
Settling time				5	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -20°C to 75°C			15	ppm
	Uncalibrated – total variation			200	ppm

3.2.13 Interrupt and Watchdog

3.2.13.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - FCHR_ENB: Interrupt is issued when FCHR_ENB is pressed (and released, set by the register). After receiving the interrupt, the software will read the FCHR_ENB _DEB status to see if it is pressed or released.
2. Thermal interrupt

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PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.

3. Charger related interrupt
4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupts.
   1) VBAT detected by AUXADC
      If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.
   2) VBAT detected by fuel gauge
      If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.
5. Fuel-Gauge
6. Buck OC interrupt
   There are 8 bucks and each has its individual interrupt which uses PWM detection method.
7. Buck PREOC interrupt
   There are 2 buck preoc interrupt for VCORE and VGPU.
8. LDO OC interrupt
   PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
9. RTC interrupt
10. AUDIO interrupt
    Audio interrupt can inform AP playback of the audio status.
11. ACCDET interrupt
    This is for headphone detection.
12. Novel Adaptive Fuel Gauge (NAFG) delta-V accumulation interrupt
    If the accumulation of NAFG delta-voltage is larger than the programmable threshold, this interrupt will be issued.

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Table 3-7. MT6351 interrupts

Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
STRUP	PWRKEY	RG_INT_EN_PWRKEY	0x02C2 bit0	RG_INT_STATUS_PWRKEY	0x02E0 bit0	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY	RG_INT_EN_HOMEKEY	0x02C2 bit1	RG_INT_STATUS_HOMEKEY	0x02E0 bit1	edge(rising & falling)	0	50ms (in STRUP)	Write 1 Clear
STRUP	PWRKEY_R	RG_INT_EN_PWRKEY_R	0x02C2 bit2	RG_INT_STATUS_PWRKEY_R	0x02E0 bit2	edge(rising)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY_R	RG_INT_EN_HOMEKEY_R	0x02C2 bit3	RG_INT_STATUS_HOMEKEY _R	0x02E0 bit3	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_H	RG_INT_EN_THR_H	0x02C2 bit4	RG_INT_STATUS_THR_H	0x02E0 bit4	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_L	RG_INT_EN_THR_L	0x02C2 bit5	RG_INT_STATUS_THR_L	0x02E0 bit5	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	BAT_H	RG_INT_EN_BAT_H	0x02C2 bit6	RG_INT_STATUS_BAT_H	0x02E0 bit6	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_L	RG_INT_EN_BAT_L	0x02C2 bit7	RG_INT_STATUS_BAT_L	0x02E0 bit7	level (high active)	0	V (in AUXADC)	Write 1 Clear
RTC	RTC	RG_INT_EN_RTC	0x02C2 bit9	RG_INT_STATUS_RTC	0x02E0 bit9	level (low active)	0	No	Write 1 Clear
Audio	AUDIO	RG_INT_EN_AUDIO	0x02C2 bit10	RG_INT_STATUS_AUDIO	0x02E0 bit10	level (high active)	0	No	Write 1 Clear
Audio	MAD	RG_INT_EN_MAD	0x02C2 bit11	RG_INT_STATUS_MAD	0x02E0 bit11	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET	RG_INT_EN_ACCDET	0x02C2 bit12	RG_INT_STATUS_ACCDET	0x02E0 bit12	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET_EINT	RG_INT_EN_ACCDET_EINT	0x02C2 bit13	RG_INT_STATUS_ACCDET_EI NT	0x02E0 bit13	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET_NEGV	RG_INT_EN_ACCDET_NEGV	0x02C2 bit14	RG_INT_STATUS_ACCDET_N EGV	0x02E0 bit14	level (high active)	0	No	Write 1 Clear
STRUP	NI_LBAT_INT	RG_INT_EN_NI_LBAT_INT	0x02C2 bit15	RG_INT_STATUS_NI_LBAT_I NT	0x02E0 bit15	edge(rising)	0	150us (in STRUP)	Write 1 Clear

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Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
Regulator	VCORE_OC	RG_INT_EN_VCORE_OC	0x02C8 bit0	RG_INT_STATUS_VCORE_OC	0x02E2 bit0	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VGPU_OC	RG_INT_EN_VGPU_OC	0x02C8 bit1	RG_INT_STATUS_VGPU_OC	0x02E2 bit1	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VSRAM_MD_OC	RG_INT_EN_VSRAM_MD_OC	0x02C8 bit2	RG_INT_STATUS_VSRAM_MD_OC	0x02E2 bit2	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VMODEM_OC	RG_INT_EN_VMODEM_OC	0x02C8 bit3	RG_INT_STATUS_VMODEM_OC	0x02E2 bit3	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VM1_OC	RG_INT_EN_VM1_OC	0x02C8 bit4	RG_INT_STATUS_VM1_OC	0x02E2 bit4	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VS1_OC	RG_INT_EN_VS1_OC	0x02C8 bit5	RG_INT_STATUS_VS1_OC	0x02E2 bit5	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VS2_OC	RG_INT_EN_VS2_OC	0x02C8 bit6	RG_INT_STATUS_VS2_OC	0x02E2 bit6	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VPA_OC	RG_INT_EN_VPA_OC	0x02C8 bit7	RG_INT_STATUS_VPA_OC	0x02E2 bit7	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VCORE_PREOC	RG_INT_EN_VCORE_PREOC	0x02C8 bit8	RG_INT_STATUS_VCORE_PREOC	0x02E2 bit8	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VGPU_PREOC	RG_INT_EN_VGPU_PREOC	0x02C8 bit9	RG_INT_STATUS_VGPU_PREOC	0x02E2 bit9	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VSRAM_MD_PREOC	RG_INT_EN_VSRAM_MD_PREOC	0x02C8 bit10	RG_INT_STATUS_VSRAM_MD_PREOC	0x02E2 bit10	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VMODEM_PREOC	RG_INT_EN_VMODEM_PREOC	0x02C8 bit11	RG_INT_STATUS_VMODEM_PREOC	0x02E2 bit11	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VM1_PREOC	RG_INT_EN_VM1_PREOC	0x02C8 bit12	RG_INT_STATUS_VM1_PREOC	0x02E2 bit12	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VS1_PREOC	RG_INT_EN_VS1_PREOC	0x02C8 bit13	RG_INT_STATUS_VS1_PREOC	0x02E2 bit13	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
Regulator	VS2_PREOC	RG_INT_EN_VS2_PREOC	0x02C8 bit14	RG_INT_STATUS_VS2_PREOC	0x02E2 bit14	level (high active)	0	5us(in INCTRL) programmable	Write 1 Clear
LDO	LDO_OC	RG_INT_EN_LDO_OC	0x02C8 bit15	RG_INT_STATUS_LDO_OC	0x02E2 bit15	level (high active)	1	100/200/400/800us (in INTCTRL)	Write 1 Clear

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Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
AUXADC	JEITA_HOT	RG_INT_EN_JEITA_HOT	0x02CE bit0	RG_INT_STATUS_JEITA_HOT	0x02E4 bit0	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_WARM	RG_INT_EN_JEITA_WARM	0x02CE bit1	RG_INT_STATUS_JEITA_WARM	0x02E4 bit1	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_COOL	RG_INT_EN_JEITA_COOL	0x02CE bit2	RG_INT_STATUS_JEITA_COOL	0x02E4 bit2	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_COLD	RG_INT_EN_JEITA_COLD	0x02CE bit3	RG_INT_STATUS_JEITA_COLD	0x02E4 bit3	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	AUXADC_IMP	RG_INT_EN_AUXADC_IMP	0x02CE bit4	RG_INT_STATUS_AUXADC_IMP	0x02E4 bit4	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	NAG_C_DLTV	RG_INT_EN_NAG_C_DLTV	0x02CE bit5	RG_INT_STATUS_NAG_C_DLTV	0x02E4 bit5	level (high active)	0	V (in AUXADC)	Write 1 Clear
Charger	OV	RG_INT_EN_OV	0x02CE bit8	RG_INT_STATUS_OV	0x02E4 bit8	edge(rising)	1	4us (in PCHR_DIG)	Write 1 Clear
Charger	BVALID_DET	RG_INT_EN_BVALID_DET	0x02CE bit9	RG_INT_STATUS_BVALID_DET	0x02E4 bit9	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	RGS_BATON_HV	RG_INT_EN_RGS_BATON_HV	0x02CE bit10	RG_INT_STATUS_RGS_BATON_HV	0x02E4 bit10	level (high active)	1	N	Write 1 Clear
Charger	VBATON_UNDET	RG_INT_EN_VBATON_UNDET	0x02CE bit11	RG_INT_STATUS_VBATON_UNDET	0x02E4 bit11	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	WATCHDOG	RG_INT_EN_WATCHDOG	0x02CE bit12	RG_INT_STATUS_WATCHDOG	0x02E4 bit12	level (high active)	1	N	Write 1 Clear
Charger	PCHR_CM_VDEC	RG_INT_EN_PCHR_CM_VDEC	0x02CE bit13	RG_INT_STATUS_PCHR_CM_VDEC	0x02E4 bit13	edge(rising)	0	N	Write 1 Clear
Charger	CHRDET	RG_INT_EN_CHRDET	0x02CE bit14	RG_INT_STATUS_CHRDET	0x02E4 bit14	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
Charger	PCHR_CM_VINC	RG_INT_EN_PCHR_CM_VINC	0x02CE bit15	RG_INT_STATUS_PCHR_CM_VINC	0x02E4 bit15	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT_H	RG_INT_EN_FG_BAT_H	0x02D4 bit0	RG_INT_STATUS_FG_BAT_H	0x02E6 bit0	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT_L	RG_INT_EN_FG_BAT_L	0x02D4 bit1	RG_INT_STATUS_FG_BAT_L	0x02E6 bit1	edge(rising)	0	N	Write 1 Clear

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Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
FGADC	FG_CUR_H	RG_INT_EN_FG_CUR_H	0x02D4 bit2	RG_INT_STATUS_FG_CUR_H	0x02E6 bit2	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CUR_L	RG_INT_EN_FG_CUR_L	0x02D4 bit3	RG_INT_STATUS_FG_CUR_L	0x02E6 bit3	edge(rising)	0	N	Write 1 Clear
FGADC	FG_ZCV	RG_INT_EN_FG_ZCV	0x02D4 bit4	RG_INT_STATUS_FG_ZCV	0x02E6 bit4	edge(rising)	0	N	Write 1 Clear

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3.2.13.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.14 SPI Interface

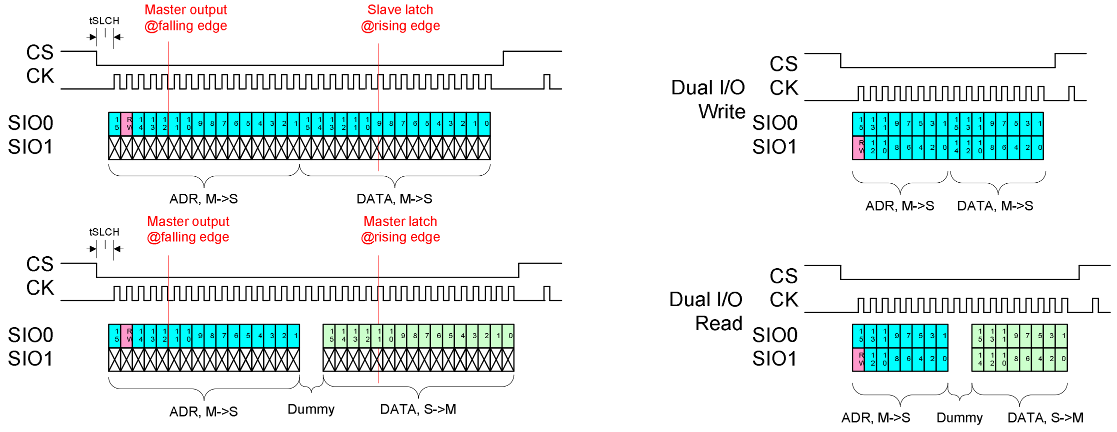
PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.14.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit 15 to bit 1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



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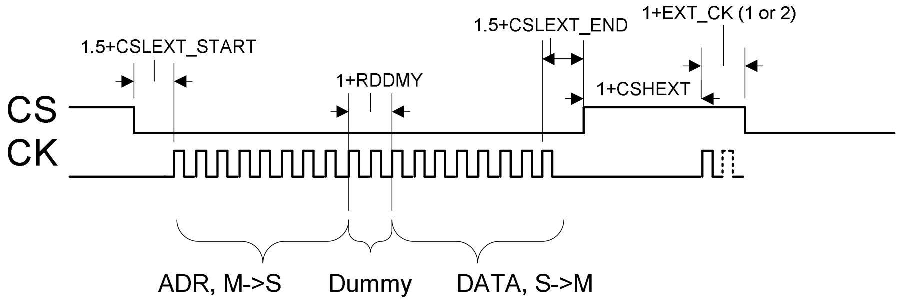
SPI parameter configuration:



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3.2.15 GPIO

3.2.15.1 GPIO List

Table 3-8. MT6351 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
PAD_SRCLKEN_IN0	GPIO0	**I1: SRCLKEN_IN0**			I0: TEST_IN0	O: TEST_OUT0	PU/PD
PAD_SRCLKEN_IN1	GPIO1	**I1: SRCLKEN_IN1**			I0: TEST_IN1	O: TEST_OUT1	PU/PD
PAD_RTC32K_1V8_0	GPIO2	**O: RTC_32K1V8_0**		I0: TEST_CK0			PU/PD
PAD_RTC32K_1V8_1	GPIO3	**O: RTC_32K1V8_1**	O: INT_1	I0: TEST_CK2	I0: TEST_IN2	O: TEST_OUT2	PU/PD
PAD_SPI_CLK	GPIO4	**I0: SPI_CLK**					PU/PD
PAD_SPI_CSN	GPIO5	**I1: SPI_CSN**					PU/PD
PAD_SPI_MOSI	GPIO6	**B0: SPI_MOSI**					PU/PD
PAD_SPI_MISO	GPIO7	**B0: SPI_MISO**					PU/PD
PAD_AUD_CLK	GPIO8	**I0: AUD_CLK**		I0: TEST_CK1			PU/PD
PAD_AUD_DAT_MOSI	GPIO9	**I0: AUD_DAT_MOSI**	O: MAD_DAT_MISO_0		I0: TEST_IN3	O: TEST_OUT3	PU/PD
PAD_AUD_DAT_MISO	GPIO10	**O: AUD_DAT_MISO**	O: MAD_DAT_MISO_1		I0: TEST_IN4	O: TEST_OUT4	PU/PD
PAD_ANC_DAT_MOSI	GPIO11	**I0: ANC_DAT_MOSI**			I0: TEST_IN5	O: TEST_OUT5	PU/PD
PAD_VOW_CLK_MISO	GPIO12	**O: VOW_CLK_MISO**	O: INT_0		I0: TEST_IN6	O: TEST_OUT6	PU/PD
PAD_ENBB	GPIO13	**O: ENBB**			I0: TEST_IN7	O: TEST_OUT7	PU/PD
PAD_XOSC_EN	GPIO14	**O: XOSC_EN**					PU/PD

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3.2.15.2 GPIO Specification

Table 3-9. MT6351 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.65*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH(DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL(DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	µA
IOZ	Tri-state output leakage current	-5		5	µA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	µA
IOZ	Tri-state output leakage current for for floating nwell IO	-10		10	µA

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3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
0000	STRUP_CON0	16	STRUP Control Register 0
0018	STRUP_CON12	16	STRUP Control Register 12
001A	STRUP_CON13	16	STRUP Control Register 13
002E	STRUP_CON23	16	STRUP Control Register 23
0030	STRUP_ANA_CON0	16	STRUP_ANA Control Register 0
0032	STRUP_ANA_CON1	16	STRUP_ANA Control Register 1
0206	TEST_OUT	16	TEST_OUT
020E	EN_STATUS1	16	Regulator Status 1
0210	EN_STATUS2	16	Regulator Status 2
0216	PGDEBSTATUS0	16	Power Good Debounce Status 0
0218	PGDEBSTATU1	16	Power Good Debounce Status 1
021A	PGSTATUS0	16	Power Good Status0
021C	PGSTATUS1	16	Power Good Status1
0220	TOPSTATUS	16	TOP Status
0222	TDSEL_CON	16	TDSEL_CON
0224	RDSEL_CON	16	RDSEL_CON
0226	SMT_CON0	16	SMT_CON0
0228	SMT_CON1	16	SMT_CON1
022A	SMT_CON2	16	SMT_CON2
022C	DRV_CON0	16	DRV_CON0
022E	DRV_CON1	16	DRV_CON1
0230	DRV_CON2	16	DRV_CON2
0232	DRV_CON3	16	DRV_CON3
0234	TOP_STATUS	16	TOP_STATUS
023A	TOP_CKPDN_CON0	16	TOP_CKPDN control Register 0
023C	TOP_CKPDN_CON0_SET	16	TOP_CKPDN_CON0 Register SET
023E	TOP_CKPDN_CON0_CLR	16	TOP_CKPDN_CON0 Register CLR
0240	TOP_CKPDN_CON1	16	TOP_CKPDN control Register 1
0242	TOP_CKPDN_CON1_SET	16	TOP_CKPDN_CON1 Register SET
0244	TOP_CKPDN_CON1_CLR	16	TOP_CKPDN_CON1 Register CLR
0246	TOP_CKPDN_CON2	16	TOP_CKPDN control Register 2
0248	TOP_CKPDN_CON2_SET	16	TOP_CKPDN_CON2 Register SET
024A	TOP_CKPDN_CON2_CLR	16	TOP_CKPDN_CON2 Register CLR
024C	TOP_CKPDN_C	16	TOP_CKPDN Control Register 3

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Address	Name	Width	Register Function
	ON3		
024E	TOP_CKPDN_CON3_SET	16	TOP_CKPDN_CON3 Register SET
0250	TOP_CKPDN_CON3_CLR	16	TOP_CKPDN_CON3 Register CLR
0252	TOP_CKPDN_CON4	16	TOP_CKPDN Control Register 4
0254	TOP_CKPDN_CON4_SET	16	TOP_CKPDN_CON4 Register SET
0256	TOP_CKPDN_CON4_CLR	16	TOP_CKPDN_CON4 Register CLR
0258	TOP_CKPDN_CON5	16	TOP_CKPDN Control Register 5
025A	TOP_CKPDN_CON5_SET	16	TOP_CKPDN_CON5 Register SET
025C	TOP_CKPDN_CON5_CLR	16	TOP_CKPDN_CON5 Register CLR
025E	TOP_CKSEL_CON0	16	TOP_CKSEL control Register 0
0260	TOP_CKSEL_CON0_SET	16	TOP_CKSEL_CON0 Register SET
0262	TOP_CKSEL_CON0_CLR	16	TOP_CKSEL_CON0 Register CLR
0264	TOP_CKSEL_CON1	16	TOP_CKSEL Control Register 1
0266	TOP_CKSEL_CON1_SET	16	TOP_CKSEL_CON1 Register SET
0268	TOP_CKSEL_CON1_CLR	16	TOP_CKSEL_CON1 Register CLR
026A	TOP_CKSEL_CON2	16	TOP_CKSEL Control Register 2
026C	TOP_CKSEL_CON2_SET	16	TOP_CKSEL_CON2 Register SET
026E	TOP_CKSEL_CON2_CLR	16	TOP_CKSEL_CON2 Register CLR
0276	TOP_CKDIVSEL_CON0	16	TOP_CKDIVSEL Control Register 0
0278	TOP_CKDIVSEL_CON0_SET	16	TOP_CKDIVSEL_CON0 Register SET
027A	TOP_CKDIVSEL_CON0_CLR	16	TOP_CKDIVSEL_CON0 Register CLR
027C	TOP_CKDIVSEL_CON1	16	TOP_CKDIVSEL Control Register 1
027E	TOP_CKDIVSEL_CON1_SET	16	TOP_CKDIVSEL_CON1 Register SET
0280	TOP_CKDIVSEL_CON1_CLR	16	TOP_CKDIVSEL_CON1 Register CLR
0282	TOP_CKHWEN_CON0	16	TOP_CKHWEN Control Register 0
0284	TOP_CKHWEN_CON0_SET	16	TOP_CKHWEN_CON0 Register SET
0286	TOP_CKHWEN_CON0_CLR	16	TOP_CKHWEN_CON0 Register CLR
0288	TOP_CKHWEN_CON1	16	TOP_CKHWEN Control Register 1

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Address	Name	Width	Register Function
028A	TOP_CKHWEN_CON1_SET	16	TOP_CKHWEN_CON1 Register SET
028C	TOP_CKHWEN_CON1_CLR	16	TOP_CKHWEN_CON1 Register CLR
028E	TOP_CKHWEN_CON2	16	TOP_CKHWEN control register 2
0290	TOP_CKHWEN_CON2_SET	16	TOP_CKHWEN_CON2 Register SET
0292	TOP_CKHWEN_CON2_CLR	16	TOP_CKHWEN_CON2 Register CLR
029A	TOP_CLKSQ	16	TOP_CLKSQ Register
029C	TOP_CLKSQ_SET	16	TOP_CLKSQ Register SET
029E	TOP_CLKSQ_CLR	16	TOP_CLKSQ Register CLR
02A0	TOP_CLKSQ_RTC	16	TOP_CLKSQ_RTC Register
02A2	TOP_CLKSQ_RTC_SET	16	TOP_CLKSQ_RTC Register SET
02A4	TOP_CLKSQ_RTC_CLR	16	TOP_CLKSQ_RTC Register CLR
02A6	TOP_CLK_TRIM	16	TOP_CLK_TRIM Register
02B6	TOP_RST_MISC	16	Reset Control Misc
041E	BUCK_OC_CON0	16	BUCK_OC Control Register 0
0424	BUCK_OC_CON3	16	BUCK_OC Control Register 3
0426	BUCK_OC_CON4	16	BUCK_OC Control Register 4
0438	SMPS_ANA_CON0	16	SMPS Control Register 0
044C	SMPS_ANA_CON10	16	SMPS Control Register 10
044E	VCORE_ANA_CON0	16	VCORE Control Register 0
0460	VCORE_ANA_CON9	16	VCORE Control Register 9
0462	VGPU_ANA_CON0	16	VGPU Control Register 0
0474	VGPU_ANA_CON9	16	VGPU Control Register 9
0476	VSRAM_MD_ANA_CON0	16	VSRAM_MD Control Register 0
0488	VSRAM_MD_ANA_CON9	16	VSRAM_MD Control Register 9
048A	VMODEM_ANA_CON0	16	VMODEM Control Register 0
049C	VMODEM_ANA_CON9	16	VMODEM Control Register 9
049E	VMD1_ANA_CON0	16	VMD1 Control Register 0
04B0	VMD1_ANA_CON9	16	VMD1 Control Register 9

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Address	Name	Width	Register Function
04B2	VS1_ANA_CON0	16	VS1 Control Register 0
04C4	VS1_ANA_CON9	16	VS1 Control Register 9
04C6	VS2_ANA_CON0	16	VS2 Control Register 0
04D8	VS2_ANA_CON9	16	VS2 Control Register 9
04DA	VPA_ANA_CON0	16	VPA Control Register 0
04E4	VPA_ANA_CON5	16	VPA Control Register 5
0608	BUCK_VCORE_CON4	16	BUCK_VCORE Control Register 4
060A	BUCK_VCORE_CON5	16	BUCK_VCORE Control Register 5
061C	BUCK_VGPU_CON4	16	BUCK_VGPU Control Register 4
061E	BUCK_VGPU_CON5	16	BUCK_VGPU Control Register 5
0630	BUCK_VMODEM_CON4	16	BUCK_VMODEM Control Register 4
0632	BUCK_VMODEM_CON5	16	BUCK_VMODEM Control Register 5
0644	BUCK_VMD1_CON4	16	BUCK_VMD1 Control Register 4
0646	BUCK_VMD1_CON5	16	BUCK_VMD1 Control Register 5
0658	BUCK_VSRAM_MD_CON4	16	BUCK_VSRAM_MD Control Register 4
065A	BUCK_VSRAM_MD_CON5	16	BUCK_VSRAM_MD Control Register 5
066C	BUCK_VS1_CON4	16	BUCK_VS1 Control Register 4
066E	BUCK_VS1_CON5	16	BUCK_VS1 Control Register 5
0680	BUCK_VS2_CON4	16	BUCK_VS2 Control Register 4
0682	BUCK_VS2_CON5	16	BUCK_VS2 Control Register 5
0690	BUCK_VPA_CON2	16	BUCK_VPA Control Register 2
0694	BUCK_VPA_CON4	16	BUCK_VPA Control Register 4
0696	BUCK_VPA_CON5	16	BUCK_VPA Control Register 5
06A8	BUCK_VSRAM_PROC_CON4	16	BUCK_VSRAM_PROC Control Register 4
0800	ZCD_CON0	16	ZCD Control Register 0
0802	ZCD_CON1	16	ZCD Control Register 1
0804	ZCD_CON2	16	ZCD Control Register 2
0806	ZCD_CON3	16	ZCD Control Register 3
0808	ZCD_CON4	16	ZCD Control Register 4
080A	ZCD_CON5	16	ZCD Control Register 5
0810	ISINK0_CON0	16	ISINK0 Control Register 0

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Address	Name	Width	Register Function
0812	ISINK0_CON1	16	ISINK0 Control Register 1
0814	ISINK0_CON2	16	ISINK0 Control Register 2
0816	ISINK0_CON3	16	ISINK0 Control Register 3
0818	ISINK1_CON0	16	ISINK1 Control Register 0
081A	ISINK1_CON1	16	ISINK1 Control Register 1
081C	ISINK1_CON2	16	ISINK1 Control Register 2
081E	ISINK1_CON3	16	ISINK1 Control Register 3
0820	ISINK4_CON0	16	ISINK4 Control Register 0
0822	ISINK4_CON1	16	ISINK4 Control Register 1
0824	ISINK4_CON2	16	ISINK4 Control Register 2
0826	ISINK4_CON3	16	ISINK4 Control Register 3
0828	ISINK5_CON0	16	ISINK5 Control Register 0
082A	ISINK5_CON1	16	ISINK5 Control Register 1
082C	ISINK5_CON2	16	ISINK5 Control Register 2
082E	ISINK5_CON3	16	ISINK5 Control Register 3
0834	ISINK_SFSTR	16	ISINK Soft Start
0836	ISINK_EN_CTRL	16	ISINK Enable Control
0838	ISINK_MODE_CTRL	16	ISINK Mode Control
083A	ISINK_ANA_CON0	16	ISINK Control Register 0
084A	CHRIND_CON0	16	CHRIND Control Register 0
084C	CHRIND_CON1	16	CHRIND Control Register 1
084E	CHRIND_CON2	16	CHRIND Control Register 2
0850	CHRIND_CON3	16	CHRIND Control Register 3
0852	CHRIND_EN_CTRL	16	CHRIND Enable Control Simple
0A00	LDO_VA18_CON0	16	LDO VA18 Control Register 0
0A02	LDO_VA18_CON1	16	LDO VA18 Control Register 1
0A04	LDO_VTCXO24_CON0	16	LDO VTCXO24 Control Register 0
0A06	LDO_VTCXO24_CON1	16	LDO VTCXO24 Control Register 1
0A08	LDO_VTCXO28_CON0	16	LDO VTCXO28 Control Register 0
0A0A	LDO_VTCXO28_CON1	16	LDO VTCXO28 Control Register 1
0A0C	LDO_VCN28_CON0	16	LDO VCN28 Control Register 0
0A0E	LDO_VCN28_CON1	16	LDO VCN28 Control Register 1
0A12	LDO_VCAMA_CON0	16	LDO VCAMA Control Register 0
0A14	LDO_VCAMA_CON1	16	LDO VCAMA Control Register 1
0A16	LDO_VUSB33_CON0	16	LDO VUSB33 Control Register 0
0A18	LDO_VUSB33_C	16	LDO VUSB33 Control Register 1

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Address	Name	Width	Register Function
	ON1		
0A1C	LDO_VSIM1_CON0	16	LDO VSIM1 Control Register 0
0A1E	LDO_VSIM1_CON1	16	LDO VSIM1 Control Register 1
0A22	LDO_VSIM2_CON0	16	LDO VSIM2 Control Register 0
0A24	LDO_VSIM2_CON1	16	LDO VSIM2 Control Register 1
0A28	LDO_VEMC_CON0	16	LDO VEMC Control Register 0
0A2A	LDO_VEMC_CON1	16	LDO VEMC Control Register 1
0A2E	LDO_VMCH_CON0	16	LDO VMCH Control Register 0
0A30	LDO_VMCH_CON1	16	LDO VMCH Control Register 1
0A34	LDO_VIO28_CON0	16	LDO VIO28 Control Register 0
0A36	LDO_VIO28_CON1	16	LDO VIO28 Control Register 1
0A3A	LDO_VIBR_CON0	16	LDO VIBR Control Register 0
0A3C	LDO_VIBR_CON1	16	LDO VIBR Control Register 1
0A40	LDO_VCAMD_CON0	16	LDO VCAMD Control Register 0
0A42	LDO_VCAMD_CON1	16	LDO VCAMD Control Register 1
0A46	LDO_VRF18_CON0	16	LDO VRF18 Control Register 0
0A48	LDO_VRF18_CON1	16	LDO VRF18 Control Register 1
0A4C	LDO_VIO18_CON0	16	LDO VIO18 Control Register 0
0A4E	LDO_VIO18_CON1	16	LDO VIO18 Control Register 1
0A52	LDO_VCN18_CON0	16	LDO VCN18 Control Register 0
0A54	LDO_VCN18_CON1	16	LDO VCN18 Control Register 1
0A58	LDO_VCAMIO_CON0	16	LDO VCAMIO Control Register 0
0A5A	LDO_VCAMIO_CON1	16	LDO VCAMIO Control Register 1
0A5E	LDO_VSRAM_PROC_CON0	16	LDO VSRAM_PROC Control Register 0
0A60	LDO_VSRAM_PROC_CON1	16	LDO VSRAM_PROC Control Register 1
0A64	LDO_VXO22_CON0	16	LDO VXO22 Control Register 0
0A66	LDO_VXO22_CON1	16	LDO VXO22 Control Register 1
0A68	LDO_VRF12_CON0	16	LDO VRF12 Control Register 0

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Address	Name	Width	Register Function
0A6A	LDO_VRF12_CON1	16	LDO VRF12 Control Register 1
0A6E	LDO_VA10_CON0	16	LDO VA10 Control Register 0
0A70	LDO_VA10_CON1	16	LDO VA10 Control Register 1
0A74	LDO_VDRAM_CON0	16	LDO VDRAM Control Register 0
0A76	LDO_VDRAM_CON1	16	LDO VDRAM Control Register 1
0A7A	LDO_VMIPI_CON0	16	LDO VMIPI Control Register 0
0A7C	LDO_VMIPI_CON1	16	LDO VMIPI Control Register 1
0A80	LDO_VGP3_CON0	16	LDO VGP3 Control Register 0
0A82	LDO_VGP3_CON1	16	LDO VGP3 Control Register 1
0A86	LDO_VBIF28_CON0	16	LDO VBIF28 Control Register 0
0A88	LDO_VBIF28_CON1	16	LDO VBIF28 Control Register 1
0A8C	LDO_VEFUSE_CON0	16	LDO VEFUSE Control Register 0
0A8E	LDO_VEFUSE_CON1	16	LDO VEFUSE Control Register 1
0A92	LDO_VCN33_CON0	16	LDO VCN33 Control Register 0
0A94	LDO_VCN33_CON1	16	LDO VCN33 Control Register 1
0A9C	LDO_VLDO28_CON0	16	LDO VLDO28 Control Register 0
0A9E	LDO_VLDO28_CON1	16	LDO VLDO28 Control Register 1
0AAA	LDO_VMC_CON0	16	LDO VMC Control Register 0
0AAC	LDO_VMC_CON1	16	LDO VMC Control Register 1
0AB0	LDO_VMC_CON3	16	LDO VMC Control Register 3
0ABA	VRTC_CON0	16	VRTC Control Register 0
0AC4	VXO22_ANA_CON0	16	VXO22 Control Register 0
0AC6	VTCXO28_ANA_CON0	16	VTCXO28 Control Register 0
0AC8	VTCXO24_ANA_CON0	16	VTCXO24 Control Register 0
0ACA	VBIF28_ANA_CON0	16	VBIF28 Control Register 0
0ACC	VCN28_ANA_CON0	16	VCN28 Control Register 0
0ACE	VMCH_ANA_CON0	16	VMCH Control Register 0
0AD0	VMCH_ANA_CON1	16	VMCH Control Register 1

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Address	Name	Width	Register Function
0AD2	VEMC_ANA_CON0	16	VEMC Control Register 0
0AD4	VEMC_ANA_CON1	16	VEMC Control Register 1
0AD6	VCAMA_ANA_CON0	16	VCAMA Control Register 0
0AD8	VCAMA_ANA_CON1	16	VCAMA Control Register 1
0ADA	VCN33_ANA_CON0	16	VCN33 Control Register 0
0ADC	VCN33_ANA_CON1	16	VCN33 Control Register 1
0ADE	VIO28_ANA_CON0	16	VIO28 Control Register 0
0AE0	VIO28_ANA_CON1	16	VIO28 Control Register 1
0AE2	VMC_ANA_CON0	16	VMC Control Register 0
0AE4	VMC_ANA_CON1	16	VMC Control Register 1
0AE6	VIBR_ANA_CON0	16	VIBR Control Register 0
0AE8	VIBR_ANA_CON1	16	VIBR Control Register 1
0AEA	VUSB33_ANA_CON0	16	VUSB33 Control Register 0
0AEC	VUSB33_ANA_CON1	16	VUSB33 Control Register 1
0AEE	VSIM1_ANA_CON0	16	VSIM1 Control Register 0
0AF0	VSIM1_ANA_CON1	16	VSIM1 Control Register 1
0AF2	VSIM2_ANA_CON0	16	VSIM2 Control Register 0
0AF4	VSIM2_ANA_CON1	16	VSIM2 Control Register 1
0AF6	VEFUSE_ANA_CON0	16	VEFUSE Control Register 0
0AF8	VEFUSE_ANA_CON1	16	VEFUSE Control Register 1
0AFA	VA18_ANA_CON0	16	VA18 Control Register 0
0AFC	VGP3_ANA_CON0	16	VGP3 Control Register 0
0AFE	VGP3_ANA_CON1	16	VGP3 Control Register 1
0B00	VCAMD_ANA_CON0	16	VCAMD Control Register 0
0B02	VCAMD_ANA_CON1	16	VCAMD Control Register 1
0B04	VIO18_ANA_CON0	16	VIO18 Control Register 0
0B06	VIO18_ANA_CON1	16	VIO18 Control Register 1
0B08	VRF18_ANA_CO	16	VRF18 Control Register 0

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Address	Name	Width	Register Function
	No		
0B0A	VRF18_ANA_CON1	16	VRF18 Control Register 1
0B0C	VRF12_ANA_CON0	16	VRF12 Control Register 0
0B0E	VRF12_ANA_CON1	16	VRF12 Control Register 1
0B10	VA10_ANA_CON0	16	VA10 Control Register 0
0B12	VA10_ANA_CON1	16	VA10 Control Register 1
0B14	VCAMIO_ANA_CON0	16	VCAMIO Control Register 0
0B16	VCAMIO_ANA_CON1	16	VCAMIO Control Register 1
0B18	VCN18_ANA_CON0	16	VCN18 Control Register 0
0B1A	VCN18_ANA_CON1	16	VCN18 Control Register 1
0B1C	VMIPI_ANA_CON0	16	VMIPI Control Register 0
0B1E	VMIPI_ANA_CON1	16	VMIPI Control Register 1
0B20	VSRAM_PROC_ANA_CON1	16	VSRAM_PROC Control Register 1
0B22	VDRAM_ANA_CON0	16	VDRAM Control Register 0
0B24	VDRAM_ANA_CON1	16	VDRAM Control Register 1
0B26	VLDO28_ANA_CON0	16	VLDO28 Control Register 0
0B28	VLDO28_ANA_CON1	16	VLDO28 Control Register 1
0B2A	BIF_CON0	16	BIF Control Register 0
0B2C	BIF_CON1	16	BIF Control Register 1
0B2E	BIF_CON2	16	BIF Control Register 2
0B30	BIF_CON3	16	BIF Control Register 3
0B32	BIF_CON4	16	BIF Control Register 4
0B34	BIF_CON5	16	BIF Control Register 5
0B36	BIF_CON6	16	BIF Control Register 6
0B38	BIF_CON7	16	BIF Control Register 7
0B3A	BIF_CON8	16	BIF Control Register 8
0B3C	BIF_CON9	16	BIF Control Register 9
0B3E	BIF_CON10	16	BIF Control Register 10
0B40	BIF_CON11	16	BIF Control Register 11
0B42	BIF_CON12	16	BIF Control Register 12
0B44	BIF_CON13	16	BIF Control Register 13
0B46	BIF_CON14	16	BIF Control Register 14
0B48	BIF_CON15	16	BIF Control Register 15
0B4A	BIF_CON16	16	BIF Control Register 16
0B4C	BIF_CON17	16	BIF Control Register 17

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Address	Name	Width	Register Function
0B4E	**BIF_CON18**	16	BIF Control Register 18
0B50	**BIF_CON19**	16	BIF Control Register 19
0B52	**BIF_CON20**	16	BIF Control Register 20
0B54	**BIF_CON21**	16	BIF Control Register 21
0B56	**BIF_CON22**	16	BIF Control Register 22
0B58	**BIF_CON23**	16	BIF Control Register 23
0B5A	**BIF_CON24**	16	BIF Control Register 24
0B5C	**BIF_CON25**	16	BIF Control Register 25
0B5E	**BIF_CON26**	16	BIF Control Register 26
0B60	**BIF_CON27**	16	BIF Control Register 27
0B62	**BIF_CON28**	16	BIF Control Register 28
0B64	**BIF_CON29**	16	BIF Control Register 29
0B68	**BIF_CON31**	16	BIF Control Register 31
0B6A	**BIF_CON32**	16	BIF Control Register 32
0B74	**BIF_BAT_CON0**	16	BIF_BATON Control Register 0
0B76	**BIF_CON37**	16	BIF Control Register 37
0B78	**BIF_CON38**	16	BIF Control Register 38
0C00	**OTP_CON0**	16	OTP Control Register 0
0C02	**OTP_CON1**	16	OTP Control Register 1
0C04	**OTP_CON2**	16	OTP Control Register 2
0C06	**OTP_CON3**	16	OTP Control Register 3
0C08	**OTP_CON4**	16	OTP Control Register 4
0C0A	**OTP_CON5**	16	OTP Control Register 5
0C0C	**OTP_CON6**	16	OTP Control Register 6
0C0E	**OTP_CON7**	16	OTP Control Register 7
0C10	**OTP_CON8**	16	OTP Control Register 8
0C12	**OTP_CON9**	16	OTP Control Register 9
0C14	**OTP_CON10**	16	OTP Control Register 10
0C16	**OTP_CON11**	16	OTP Control Register 11
0C18	**OTP_CON12**	16	OTP Control Register 12
0C1A	**OTP_CON13**	16	OTP Control Register 13
0C1C	**OTP_CON14**	16	OTP Control Register 14
0C1E	**OTP_DOUT_0_15**	16	OTP dout 0 15
0C20	**OTP_DOUT_16_31**	16	OTP dout 16 31
0C22	**OTP_DOUT_32_47**	16	OTP dout 32 47
0C24	**OTP_DOUT_48_63**	16	OTP dout 48 63
0C26	**OTP_DOUT_64_79**	16	OTP dout 64 79
0C28	**OTP_DOUT_80_95**	16	OTP dout 80 95
0C2A	**OTP_DOUT_96_111**	16	OTP dout 96 111
0C2C	**OTP_DOUT_112_127**	16	OTP dout 112 127

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Address	Name	Width	Register Function
0C2E	**OTP_DOUT_128_143**	16	OTP dout 128 143
0C30	**OTP_DOUT_144_159**	16	OTP dout 144 159
0C32	**OTP_DOUT_160_175**	16	OTP dout 160 175
0C34	**OTP_DOUT_176_191**	16	OTP dout 176 191
0C36	**OTP_DOUT_192_207**	16	OTP dout 192 207
0C38	**OTP_DOUT_208_223**	16	OTP dout 208 223
0C3A	**OTP_DOUT_224_239**	16	OTP dout 224 239
0C3C	**OTP_DOUT_240_255**	16	OTP dout 240 255
0C3E	**OTP_DOUT_256_271**	16	OTP dout 256 271
0C40	**OTP_DOUT_272_287**	16	OTP dout 272 287
0C42	**OTP_DOUT_288_303**	16	OTP dout 288 303
0C44	**OTP_DOUT_304_319**	16	OTP dout 304 319
0C46	**OTP_DOUT_320_335**	16	OTP dout 320 335
0C48	**OTP_DOUT_336_351**	16	OTP dout 336 351
0C4A	**OTP_DOUT_352_367**	16	OTP dout 352 367
0C4C	**OTP_DOUT_368_383**	16	OTP dout 368 383
0C4E	**OTP_DOUT_384_399**	16	OTP dout 384 399
0C50	**OTP_DOUT_400_415**	16	OTP dout 400 415
0C52	**OTP_DOUT_416_431**	16	OTP dout 416 431
0C54	**OTP_DOUT_432_447**	16	OTP dout 432 447
0C56	**OTP_DOUT_448_463**	16	OTP dout 448 463
0C58	**OTP_DOUT_464_479**	16	OTP dout 464 479
0C5A	**OTP_DOUT_480_495**	16	OTP dout 480 495
0C5C	**OTP_DOUT_496_511**	16	OTP dout 496 511
0C5E	**OTP_VAL_0_15**	16	OTP val 0 15
0C60	**OTP_VAL_16_31**	16	OTP val 16 31
0C62	**OTP_VAL_32_47**	16	OTP val 32 47
0C64	**OTP_VAL_48_63**	16	OTP val 48 63

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Address	Name	Width	Register Function
0C66	**OTP_VAL_64_79**	16	OTP val 64 79
0C68	**OTP_VAL_80_95**	16	OTP val 80 95
0C6A	**OTP_VAL_96_111**	16	OTP val 96 111
0C6C	**OTP_VAL_112_127**	16	OTP val 112 127
0C6E	**OTP_VAL_128_143**	16	OTP val 128 143
0C70	**OTP_VAL_144_159**	16	OTP val 144 159
0C72	**OTP_VAL_160_175**	16	OTP val 160 175
0C74	**OTP_VAL_176_191**	16	OTP val 176 191
0C76	**OTP_VAL_192_207**	16	OTP val 192 207
0C78	**OTP_VAL_208_223**	16	OTP val 208 223
0C7A	**OTP_VAL_224_239**	16	OTP val 224 239
0C7C	**OTP_VAL_240_255**	16	OTP val 240 255
0C7E	**OTP_VAL_256_271**	16	OTP val 256 271
0C80	**OTP_VAL_272_287**	16	OTP val 272 287
0C82	**OTP_VAL_288_303**	16	OTP val 288 303
0C84	**OTP_VAL_304_319**	16	OTP val 304 319
0C86	**OTP_VAL_320_335**	16	OTP val 320 335
0C88	**OTP_VAL_336_351**	16	OTP val 336 351
0C8A	**OTP_VAL_352_367**	16	OTP val 352 367
0C8C	**OTP_VAL_368_383**	16	OTP val 368 383
0C8E	**OTP_VAL_384_399**	16	OTP val 384 399
0C90	**OTP_VAL_400_415**	16	OTP val 400 415
0C92	**OTP_VAL_416_431**	16	OTP val 416 431
0C94	**OTP_VAL_432_447**	16	OTP val 432 447
0C96	**OTP_VAL_448_463**	16	OTP val 448 463
0C98	**OTP_VAL_464_479**	16	OTP val 464 479
0C9A	**OTP_VAL_480_495**	16	OTP val 480 495
0C9C	**OTP_VAL_496_**	16	OTP val 496 511

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Address	Name	Width	Register Function
	511		
0CA6	FGADC_CON1	16	FGADC Control Register 1
0CA8	FGADC_CON2	16	FGADC Control Register 2
0CAA	FGADC_CON3	16	FGADC Control Register 3
0CAC	FGADC_CON4	16	FGADC Control Register 4
0CAE	FGADC_CON5	16	FGADC Control Register 5
0CB0	FGADC_CON6	16	FGADC Control Register 6
0CBA	FGADC_CON11	16	FGADC Control Register 11
0CC0	FGADC_CON14	16	FGADC Control Register 14
0CF2	AUDDEC_ANA_CON0	16	AUDDEC Control Register 0
0CF4	AUDDEC_ANA_CON1	16	AUDDEC Control Register 1
0CF6	AUDDEC_ANA_CON2	16	AUDDEC Control Register 2
0CF8	AUDDEC_ANA_CON3	16	AUDDEC Control Register 3
0CFA	AUDDEC_ANA_CON4	16	AUDDEC Control Register 4
0CFC	AUDDEC_ANA_CON5	16	AUDDEC Control Register 5
0CFE	AUDDEC_ANA_CON6	16	AUDDEC Control Register 6
0D00	AUDDEC_ANA_CON7	16	AUDDEC Control Register 7
0D02	AUDDEC_ANA_CON8	16	AUDDEC Control Register 8
0D04	AUDDEC_ANA_CON9	16	AUDDEC Control Register 9
0D06	AUDDEC_ANA_CON10	16	AUDDEC Control Register 10
0D08	AUDENC_ANA_CON0	16	AUDENC Control Register 0
0D0A	AUDENC_ANA_CON1	16	AUDENC Control Register 1
0D0C	AUDENC_ANA_CON2	16	AUDENC Control Register 2
0D0E	AUDENC_ANA_CON3	16	AUDENC Control Register 3
0D10	AUDENC_ANA_CON4	16	AUDENC Control Register 4
0D12	AUDENC_ANA_CON5	16	AUDENC Control Register 5
0D14	AUDENC_ANA_CON6	16	AUDENC Control Register 6
0D16	AUDENC_ANA_CON7	16	AUDENC Control Register 7
0D18	AUDENC_ANA_CON8	16	AUDENC Control Register 8
0D1A	AUDENC_ANA_CON9	16	AUDENC Control Register 9
0D1C	AUDENC_ANA_CON10	16	AUDENC Control Register 10

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Address	Name	Width	Register Function
0D1E	AUDENC_ANA_CON11	16	AUDENC Control Register 11
0D20	AUDENC_ANA_CON12	16	AUDENC Control Register 12
0D22	AUDENC_ANA_CON13	16	AUDENC Control Register 13
0D24	AUDENC_ANA_CON14	16	AUDENC Control Register 14
0D26	AUDENC_ANA_CON15	16	AUDENC Control Register 15
0D28	AUDENC_ANA_CON16	16	AUDENC Control Register 16
0D2A	AUDNCP_CLKDIV_CON0	16	AUDNCP_CLKDIV Control Register 0
0D2C	AUDNCP_CLKDIV_CON1	16	AUDNCP_CLKDIV Control Register 1
0D2E	AUDNCP_CLKDIV_CON2	16	AUDNCP_CLKDIV Control Register 2
0D30	AUDNCP_CLKDIV_CON3	16	AUDNCP_CLKDIV Control Register 3
0D32	AUDNCP_CLKDIV_CON4	16	AUDNCP_CLKDIV Control Register 4
0E00	AUXADC_ADC0	16	AUXADC ADC Register 0
0E02	AUXADC_ADC1	16	AUXADC ADC Register 1
0E04	AUXADC_ADC2	16	AUXADC ADC Register 2
0E06	AUXADC_ADC3	16	AUXADC ADC Register 3
0E08	AUXADC_ADC4	16	AUXADC ADC Register 4
0E0A	AUXADC_ADC5	16	AUXADC ADC Register 5
0E0C	AUXADC_ADC6	16	AUXADC ADC Register 6
0E0E	AUXADC_ADC7	16	AUXADC ADC Register 7
0E10	AUXADC_ADC8	16	AUXADC ADC Register 8
0E12	AUXADC_ADC9	16	AUXADC ADC Register 9
0E14	AUXADC_ADC10	16	AUXADC ADC Register 10
0E16	AUXADC_ADC11	16	AUXADC ADC Register 11
0E18	AUXADC_ADC12	16	AUXADC ADC Register 12
0E1A	AUXADC_ADC13	16	AUXADC ADC Register 13
0E1C	AUXADC_ADC14	16	AUXADC ADC Register 14
0E1E	AUXADC_ADC15	16	AUXADC ADC Register 15
0E20	AUXADC_ADC16	16	AUXADC ADC Register 16
0E22	AUXADC_ADC17	16	AUXADC ADC Register 17
0E24	AUXADC_ADC18	16	AUXADC ADC Register 18
0E26	AUXADC_ADC19	16	AUXADC ADC Register 19
0E28	AUXADC_ADC20	16	AUXADC ADC Register 20

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Address	Name	Width	Register Function
0E2A	AUXADC_ADC21	16	AUXADC ADC Register 21
0E2C	AUXADC_ADC22	16	AUXADC ADC Register 22
0E2E	AUXADC_ADC23	16	AUXADC ADC Register 23
0E30	AUXADC_ADC24	16	AUXADC ADC Register 24
0E32	AUXADC_ADC25	16	AUXADC ADC Register 25
0E34	AUXADC_ADC26	16	AUXADC ADC Register 26
0E36	AUXADC_ADC27	16	AUXADC ADC Register 27
0E38	AUXADC_ADC28	16	AUXADC ADC Register 28
0E3A	AUXADC_ADC29	16	AUXADC ADC Register 29
0E3C	AUXADC_ADC30	16	AUXADC ADC Register 30
0E3E	AUXADC_ADC31	16	AUXADC ADC Register 31
0E40	AUXADC_ADC32	16	AUXADC ADC Register 32
0E42	AUXADC_ADC33	16	AUXADC ADC Register 33
0E44	AUXADC_ADC34	16	AUXADC ADC Register 34
0E46	AUXADC_ADC35	16	AUXADC ADC Register 35
0E48	AUXADC_ADC36	16	AUXADC ADC Register 36
0E4A	AUXADC_ADC37	16	AUXADC ADC Register 37
0E4C	AUXADC_ADC38	16	AUXADC ADC Register 38
0E4E	AUXADC_ADC39	16	AUXADC ADC Register 39
0E50	AUXADC_BUF0	16	AUXADC_BUF0
0E52	AUXADC_BUF1	16	AUXADC_BUF1
0E54	AUXADC_BUF2	16	AUXADC_BUF2
0E56	AUXADC_BUF3	16	AUXADC_BUF3
0E58	AUXADC_BUF4	16	AUXADC_BUF4
0E5A	AUXADC_BUF5	16	AUXADC_BUF5
0E5C	AUXADC_BUF6	16	AUXADC_BUF6
0E5E	AUXADC_BUF7	16	AUXADC_BUF7
0E60	AUXADC_BUF8	16	AUXADC_BUF8
0E62	AUXADC_BUF9	16	AUXADC_BUF9
0E64	AUXADC_BUF10	16	AUXADC_BUF10
0E66	AUXADC_BUF11	16	AUXADC_BUF11
0E68	AUXADC_BUF12	16	AUXADC_BUF12

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Address	Name	Width	Register Function
0E6A	AUXADC_BUF13	16	AUXADC_BUF13
0E6C	AUXADC_BUF14	16	AUXADC_BUF14
0E6E	AUXADC_BUF15	16	AUXADC_BUF15
0E70	AUXADC_BUF16	16	AUXADC_BUF16
0E72	AUXADC_BUF17	16	AUXADC_BUF17
0E74	AUXADC_BUF18	16	AUXADC_BUF18
0E76	AUXADC_BUF19	16	AUXADC_BUF19
0E78	AUXADC_BUF20	16	AUXADC_BUF20
0E7A	AUXADC_BUF21	16	AUXADC_BUF21
0E7C	AUXADC_BUF22	16	AUXADC_BUF22
0E7E	AUXADC_BUF23	16	AUXADC_BUF23
0E80	AUXADC_BUF24	16	AUXADC_BUF24
0E82	AUXADC_BUF25	16	AUXADC_BUF25
0E84	AUXADC_BUF26	16	AUXADC_BUF26
0E86	AUXADC_BUF27	16	AUXADC_BUF27
0E88	AUXADC_BUF28	16	AUXADC_BUF28
0E8A	AUXADC_BUF29	16	AUXADC_BUF29
0E8C	AUXADC_BUF30	16	AUXADC_BUF30
0E8E	AUXADC_BUF31	16	AUXADC_BUF31
0E90	AUXADC_STA0	16	AUXADC_STA0
0E92	AUXADC_STA1	16	AUXADC_STA1
0E94	AUXADC_STA2	16	AUXADC_STA2
0F46	ACCDET_CON0	16	ACCDET Control Register 0
0F48	ACCDET_CON1	16	ACCDET Control Register 1
0F4A	ACCDET_CON2	16	ACCDET Control Register 2
0F4C	ACCDET_CON3	16	ACCDET Control Register 3
0F4E	ACCDET_CON4	16	ACCDET Control Register 4
0F50	ACCDET_CON5	16	ACCDET Control Register 5
0F52	ACCDET_CON6	16	ACCDET Control Register 6
0F54	ACCDET_CON7	16	ACCDET Control Register 7
0F56	ACCDET_CON8	16	ACCDET Control Register 8
0F58	ACCDET_CON9	16	ACCDET Control Register 9
0F5A	ACCDET_CON10	16	ACCDET Control Register 10
0F5E	ACCDET_CON12	16	ACCDET Control Register 12

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Address	Name	Width	Register Function
0F62	ACCDET_CON14	16	ACCDET Control Register 14
0F64	ACCDET_CON15	16	ACCDET Control Register 15
0F66	ACCDET_CON16	16	ACCDET Control Register 16
0F6A	ACCDET_CON19	16	ACCDET Control Register 19
0F78	CHR_CON0	16	Charger Control Register 0
0F7A	CHR_CON1	16	Charger Control Register 1
0F7C	CHR_CON2	16	Charger Control Register 2
0F7E	CHR_CON3	16	Charger Control Register 3
0F80	CHR_CON4	16	Charger Control Register 4
0F84	CHR_CON6	16	Charger Control Register 6
0F86	CHR_CON7	16	Charger Control Register 7
0F8A	CHR_CON9	16	Charger Control Register 9
0F8C	CHR_CON10	16	Charger Control Register 10
0F92	CHR_CON13	16	Charger Control Register 13
0F96	CHR_CON15	16	Charger Control Register 15
0F98	CHR_CON16	16	Charger Control Register 16
0F9A	CHR_CON17	16	Charger Control Register 17
0F9C	CHR_CON18	16	Charger Control Register 18
0F9E	CHR_CON19	16	Charger Control Register 19
0FA0	CHR_CON20	16	Charger Control Register 20
0FA2	CHR_CON21	16	Charger Control Register 21
0FA6	CHR_CON23	16	Charger Control Register 23
0FA8	CHR_CON24	16	Charger Control Register 24
0FAA	CHR_CON25	16	Charger Control Register 25
0FB4	CHR_CON30	16	Charger Control Register 30
0FB6	CHR_CON31	16	Charger Control Register 31
0FB8	CHR_CON32	16	Charger Control Register 32
0FBA	CHR_CON33	16	Charger Control Register 33
0FBC	CHR_CON34	16	Charger Control Register 34
0FBE	CHR_CON35	16	Charger Control Register 35
0FC0	CHR_CON36	16	Charger Control Register 36
0FC2	CHR_CON37	16	Charger Control Register 37
0FC4	CHR_CON38	16	Charger Control Register 38
0FC6	CHR_CON39	16	Charger Control Register 39
0FC8	CHR_CON40	16	Charger Control Register 40
0FCA	CHR_CON41	16	Charger Control Register 41
0FCC	CHR_CON42	16	Charger Control Register 42
0FD0	CHR_CON43	16	Charger Control Register 43
0FD2	CHR_CON44	16	Charger Control Register 44
0FD8	CHR_CON47	16	Charger Control Register 47
0FDA	CHR_CON48	16	Charger Control Register 48

0000 STRUP_CON0 STRUP Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name											**THR_HWPDN_EN**					**THR_DET_DIS**
Type											RW					RW
Reset											0					0

Bit(s)	Name	Description
5	THR_HWPDN_EN	**Enables theraml auto power-down** Powers down some PMU modules. 0: Disable 1: Enable
0	THR_DET_DIS	**Disables thermal detection function** and thermal shut-down 0: Normal mode 1: Disable thermal detection

0018 **STRUP_CON12** **STRUP Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_OSC_EN**	**JUST_PWRKEY_RST**														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_QI_OSC_EN	**Enables internal oscillator** 0: Disable 1: Enable
14	JUST_PWRKEY_RST	**Long press reset indicator**

001A **STRUP_CON13** **STRUP Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**STRUP_EXT_PMIC_SEL**	**STRUP_EXT_PMIC_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	STRUP_EXT_PMIC_SEL	**Selects QI_EXT_PMIC_EN control** 0: HW mode 1: SW mode
0	STRUP_EXT_PMIC_EN	**Enables QI_EXT_PMIC_EN software mode**

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002E **STRUP_CON23** **STRUP Control Register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_STRUP_PWRKEY_COUNT_RESET**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_STRUP_PWRKEY_COUNT_RESET	**Resets long press shut-down counter** 1'b1: Reset long press counter 1'b0: Does not reset long press counter

0030 **STRUP_ANA_CON0** **STRUP_ANA Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_PMU_RSV**				**RG_FCHR_PU_EN**		**RGS_ANA_CHIP_ID**									
Type	RW				RW		RO									
Reset	0	0	0	0	0		0	0	0							

Bit(s)	Name	Description
15:12	RG_PMU_RSV	**Reserved bits**
11	RG_FCHR_PU_EN	**Enables FCHR internal resistor pull-up** 0: Disable pull up R 1: Enable pull up R => normal key function
9:7	RGS_ANA_CHIP_ID	**Chip ID**

0032 **STRUP_ANA_CON1** **STRUP_ANA Control Register 1** **8800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VREF_BG**			**RG_STRUP_IREF_TRIM**					**RG_RST_DRVSEL**	**RG_EN_DRVSEL**	**RG_FCHR_KEYDET_EN**	
Type					RW			RW					RW	RW	RW	
Reset					1	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
11:9	RG_VREF_BG	**Reference current fine tunning to compensate bandgap (BG) voltage variation**

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Bit(s)	Name	Description
		000: VBG=1.16V 001: VBG=1.17V 010: VBG=1.18V 011: VBG=1.19V 100: VBG=1.20V (default) 101: VBG=1.21V 110: VBG=1.22V 111: VBG=1.23V
8:4	RG_STRUP_IREF_TRIM	**Reference current trimming bits, trimmming current range: 0.5uA~1.4375uA (step=31.25nA), typ=1uA** 00000: 1uA 00001~01111: +31.25nA/step 10000: 0.5uA 10001~11111: +31.25nA/step
3	RG_RST_DRVSEL	**Selects reset pin output driving capability** 0: 7.5mA (default) 1: 15mA
2	RG_EN_DRVSEL	**Selects EXT_PMIC_EN pin output driving capability** 0: 7.5mA (default) 1: 15mA
1	RG_FCHR_KEYDET_EN	**FCHR mode state hold without key press detection feature** 0: Enable 1: Disable

0206 TEST_OUT TEST_OUT 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TEST_OUT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TEST_OUT	Monitor

020E EN_STATUS1 Regulator Status 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_STATUS_VRTC	EN_STATUS_VA18	EN_STATUS_VTCXO28	EN_STATUS_VTCXO24	EN_STATUS_VCN28	EN_STATUS_VCAMA	EN_STATUS_VCN33	EN_STATUS_VUSB33	EN_STATUS_VEFUSE	EN_STATUS_VSIM1	EN_STATUS_VSIM2	EN_STATUS_VEMC	EN_STATUS_VMC	EN_STATUS_VMCH	EN_STATUS_VIO28	EN_STATUS_VLDO28
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	EN_STATUS_VRTC	0: Off 1: On
14	EN_STATUS_VA18	0: Off 1: On
13	EN_STATUS_VTCXO	0: Off

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Bit(s)	Name	Description
	28	1: On
12	EN_STATUS_VTCXO24	0: Off 1: On
11	EN_STATUS_VCN28	0: Off 1: On
10	EN_STATUS_VCAMA	0: Off 1: On
9	EN_STATUS_VCN33	0: Off 1: On
8	EN_STATUS_VUSB33	0: Off 1: On
7	EN_STATUS_VEFUSE	0: Off 1: On
6	EN_STATUS_VSIM1	0: Off 1: On
5	EN_STATUS_VSIM2	0: Off 1: On
4	EN_STATUS_VEMC	0: Off 1: On
3	EN_STATUS_VMC	0: Off 1: On
2	EN_STATUS_VMCH	0: Off 1: On
1	EN_STATUS_VIO28	0: Off 1: On
0	EN_STATUS_VLDO28	0: Off 1: On

0210 **EN_STATUS2** **Regulator Status 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EN_STATUS_VIBR**	**EN_STATUS_VCAMD**	**EN_STATUS_VRF18**	**EN_STATUS_VIO18**	**EN_STATUS_VCN18**	**EN_STATUS_VCAMIO**	**EN_STATUS_VSRAM_PROC**	**EN_STATUS_VXO22**	**EN_STATUS_VRF12**	**EN_STATUS_VA10**	**EN_STATUS_VDRAM**	**EN_STATUS_VMIPI**	**EN_STATUS_VGP3**	**EN_STATUS_VBIF28**		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	EN_STATUS_VIBR	0: Off 1: On
14	EN_STATUS_VCAMD	0: Off 1: On
13	EN_STATUS_VRF18	0: Off 1: On
12	EN_STATUS_VIO18	0: Off 1: On
11	EN_STATUS_VCN18	0: Off 1: On

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Bit(s)	Name	Description
10	EN_STATUS_VCAMIO	0: Off 1: On
9	EN_STATUS_VSRAM_PROC	0: Off 1: On
8	EN_STATUS_VXO22	0: Off 1: On
7	EN_STATUS_VRF12	0: Off 1: On
6	EN_STATUS_VA10	0: Off 1: On
5	EN_STATUS_VDRAM	0: Off 1: On
4	EN_STATUS_VMIPI	0: Off 1: On
3	EN_STATUS_VGP3	0: Off 1: On
2	EN_STATUS_VBIF28	0: Off 1: On

0216 **PGDEBSTATUS0** **Power Good Debounce Status 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**VTCXO24_PG_DEB**	**VXO22_PG_DEB**	**VUSB33_PG_DEB**	**VGPU_PG_DEB**	**VDRAM_PG_DEB**	**VSRAM_PROC_PG_DEB**	**VSRAM_MD_PG_DEB**	**VIO28_PG_DEB**	**VA10_PG_DEB**	**VEMC_PG_DEB**	**VIO18_PG_DEB**	**VS2_PG_DEB**	**VMODEM_PG_DEB**	**VMD1_PG_DEB**	**VCORE_PG_DEB**	**VA18_PG_DEB**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	VTCXO24_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
14	VXO22_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
13	VUSB33_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
12	VGPU_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
11	VDRAM_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
10	VSRAM_PROC_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
9	VSRAM_MD_PG_DE	**PG status (dynamic change with HW)**

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Bit(s)	Name	Description
	B	0: Power is not good. 1: Power is good.
8	VIO28_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
7	VA10_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
6	VEMC_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
5	VIO18_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
4	VS2_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
3	VMODEM_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
2	VMD1_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
1	VCORE_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.
0	VA18_PG_DEB	**PG status (dynamic change with HW)** 0: Power is not good. 1: Power is good.

0218 **PGDEBSTATU1** **Power Good Debounce Status 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VS1_PG_DEB															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	VS1_PG_DEB	**PG status** 0: Power is not good. 1: Power is good.

021A **PGSTATUS0** **Power Good Status 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VT	STRUP_VX	STRUP_VU	STRUP_VG	STRUP_VD	STRUP_VS	STRUP_VS	STRUP_VI	STRUP_VA	STRUP_VE	STRUP_VI	STRUP_VS	STRUP_VM	STRUP_V	STRUP_VC	STRUP_VA

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	CXO24_PG_STATUS	O22_PG_STATUS	SB33_PG_STATUS	PU_PG_STATUS	RAM_PG_STATUS	RAM_PROC_PG_STATUS	RAM_MD_PG_STATUS	O28_PG_STATUS	10_PG_STATUS	MC_PG_STATUS	O18_PG_STATUS	2_PG_STATUS	ODEM_PG_STATUS	MD1_PG_STATUS	ORE_PG_STATUS	18_PG_STATUS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	STRUP_VTCXO24_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
14	STRUP_VXO22_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
13	STRUP_VUSB33_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
12	STRUP_VGPU_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
11	STRUP_VDRAM_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
10	STRUP_VSRAM_PROC_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
9	STRUP_VSRAM_MD_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
8	STRUP_VIO28_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
7	STRUP_VA10_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
6	STRUP_VEMC_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
5	STRUP_VIO18_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
4	STRUP_VS2_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
3	STRUP_VMODEM_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
2	STRUP_VMD1_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.
1	STRUP_VCORE_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good.

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Bit(s)	Name	Description
		1: Power is good.
0	STRUP_VA18_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.

021C PGSTATUS1 Power Good Status 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**STRUP_VS1_PG_STATUS**															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	STRUP_VS1_PG_STATUS	**PG status (cleared by SW)** 0: Power is not good. 1: Power is good.

0220 TOPSTATUS TOP Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**HOMEKEY_DEB**	**PWRKEY_DEB**	
Type														RO	RO	
Reset														0	0	

Bit(s)	Name	Description
2	HOMEKEY_DEB	
1	PWRKEY_DEB	

0222 TDSEL_CON TDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RG_E32CAL_TDSEL**	**RG_AUD_TDSEL**	**RG_SPI_TDSEL**	**RG_PMU_TDSEL**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_TDSEL	TDSEL
2	RG_AUD_TDSEL	TDSEL
1	RG_SPI_TDSEL	TDSEL
0	RG_PMU_TDSEL	TDSEL

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0224 RDSEL_CON RDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_E32CAL_RDSEL	RG_AUD_RDSEL	RG_SPI_RDSEL	RG_PMU_RDSEL
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_RDSEL	RDSEL
2	RG_AUD_RDSEL	RDSEL
1	RG_SPI_RDSEL	RDSEL
0	RG_PMU_RDSEL	RDSEL

0226 SMT_CON0 SMT_CON0 003C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SMT_RTC_32K1V8_1	RG_SMT_RTC_32K1V8_0	RG_SMT_SRCLKEN_IN1	RG_SMT_SRCLKEN_IN0	RG_SMT_HOMEKEY	RG_SMT_WDTRSTB_IN
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	0	0

Bit(s)	Name	Description
5	RG_SMT_RTC_32K1V8_1	**SMT** 0: Disable 1: Enable
4	RG_SMT_RTC_32K1V8_0	**SMT** 0: Disable 1: Enable
3	RG_SMT_SRCLKEN_IN1	**SMT** 0: Disable 1: Enable
2	RG_SMT_SRCLKEN_IN0	**SMT** 0: Disable 1: Enable
1	RG_SMT_HOMEKEY	**SMT** 0: Disable 1: Enable
0	RG_SMT_WDTRSTB_IN	**SMT** 0: Disable 1: Enable

0228 SMT_CON1 SMT_CON1 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SPI_MISO	RG_SMT_SPI_MOSI	RG_SMT_SPI_CSN	RG_SMT_SPI_CLK
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_SMT_SPI_MISO	**SMT** 0: Disable 1: Enable
2	RG_SMT_SPI_MOSI	**SMT** 0: Disable 1: Enable
1	RG_SMT_SPI_CSN	**SMT** 0: Disable 1: Enable
0	RG_SMT_SPI_CLK	**SMT** 0: Disable 1: Enable

022A **SMT_CON2** **SMT_CON2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_SMT_XOSC_EN	RG_SMT_ENBB	RG_SMT_VOW_CLK_MISO	RG_SMT_ANC_DAT_MOSI	RG_SMT_AUD_DAT_MISO	RG_SMT_AUD_DAT_MOSI	RG_SMT_AUD_CLK
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	RG_SMT_XOSC_EN	**SMT** 0: Disable 1: Enable
5	RG_SMT_ENBB	**SMT** 0: Disable 1: Enable
4	RG_SMT_VOW_CLK_MISO	**SMT** 0: Disable 1: Enable
3	RG_SMT_ANC_DAT_MOSI	**SMT** 0: Disable 1: Enable
2	RG_SMT_AUD_DAT_MISO	**SMT** 0: Disable 1: Enable
1	RG_SMT_AUD_DAT_MOSI	**SMT** 0: Disable 1: Enable
0	RG_SMT_AUD_CLK	**SMT**

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Bit(s)	Name	Description
		0: Disable 1: Enable

022C **DRV_CON0** **DRV_CON0** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_RTC_32K1V8_1				RG_OCTL_RTC_32K1V8_0				RG_OCTL_SRCLKEN_IN1				RG_OCTL_SRCLKEN_IN0			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_RTC_32K1V8_1	OC CTL
11:8	RG_OCTL_RTC_32K1V8_0	OC CTL
7:4	RG_OCTL_SRCLKEN_IN1	OC CTL
3:0	RG_OCTL_SRCLKEN_IN0	OC CTL

022E **DRV_CON1** **DRV_CON1** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SPI_MISO				RG_OCTL_SPI_MOSI				RG_OCTL_SPI_CSN				RG_OCTL_SPI_CLK			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_SPI_MISO	OC CTL
11:8	RG_OCTL_SPI_MOSI	OC CTL
7:4	RG_OCTL_SPI_CSN	OC CTL
3:0	RG_OCTL_SPI_CLK	OC CTL

0230 **DRV_CON2** **DRV_CON2** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_ANC_DAT_MOSI				RG_OCTL_AUD_CLK				RG_OCTL_AUD_DAT_MISO				RG_OCTL_AUD_DAT_MOSI			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_ANC_DAT_MOSI	OC CTL
11:8	RG_OCTL_AUD_CLK	OC CTL
7:4	RG_OCTL_AUD_DAT_MISO	OC CTL

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Bit(s)	Name	Description
3:0	RG_OCTL_AUD_DAT_MOSI	OC CTL

0232 **DRV_CON3** **DRV_CON3** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_VOW_CLK_MISO				RG_OCTL_XOSC_EN				RG_OCTL_ENBB				RG_OCTL_HOMEKEY			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_VOW_CLK_MISO	OC CTL
11:8	RG_OCTL_XOSC_EN	OC CTL
7:4	RG_OCTL_ENBB	OC CTL
3:0	RG_OCTL_HOMEKEY	OC CTL

0234 **TOP_STATUS** **TOP_STATUS** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TOP_STATUS			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TOP_STATUS	

023A **TOP_CKPDN_CON0** **TOP_CKPDN Control Register 0** **DEFC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ZCD13M_CK_PDN	RG_AUD_CK_PDN	RG_AUDIF_CK_PDN	RG_AUDNCP_CK_PDN	RG_AUXADC_26M_CK_PDN	RG_AUXADC_RNG_CK_PDN	RG_AUXADC_SMPS_CK_PDN	RG_AUXADC_1M_CK_PDN	RG_DRV_ISINK3_CK_PDN	RG_DRV_ISINK2_CK_PDN	RG_DRV_ISINK1_CK_PDN	RG_DRV_ISINK0_CK_PDN	RG_DRV_32K_CK_PDN	RG_GDRV_2M_CK_PDN	RG_GSMPS_AUD_CK_PDN	RG_GSMPS_PD_CK_PDN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	0

Bit(s)	Name	Description
15	RG_ZCD13M_CK_PDN	**Powers down ZCD13M_CK** 0: Power on 1: Power down
14	RG_AUD_CK_PDN	**Powers down AUD_CK** 0: Power on 1: Power down

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Bit(s)	Name	Description
13	RG_AUDIF_CK_PDN	**Powers down AUDIF_CK** 0: Power on 1: Power down
12	RG_AUDNCP_CK_PDN	**Powers down AUDNCP_CK** 0: Power on 1: Power down
11	RG_AUXADC_26M_CK_PDN	**Powers down AUXADC_26M_CK** 0: Power on 1: Power down
10	RG_AUXADC_RNG_CK_PDN	**Powers down AUXADC_RNG_CK** 0: Power on 1: Power down
9	RG_AUXADC_SMPS_CK_PDN	**Powers down AUXADC_SMPS_CK** 0: Power on 1: Power down
8	RG_AUXADC_1M_CK_PDN	**Powers down AUXADC_1M_CK** 0: Power on 1: Power down
7	RG_DRV_ISINK3_CK_PDN	**Powers down DRV_ISINK3_CK** 0: Power on 1: Power down
6	RG_DRV_ISINK2_CK_PDN	**Powers down DRV_ISINK2_CK** 0: Power on 1: Power down
5	RG_DRV_ISINK1_CK_PDN	**Powers down DRV_ISINK1_CK** 0: Power on 1: Power down
4	RG_DRV_ISINK0_CK_PDN	**Powers down DRV_ISINK0_CK** 0: Power on 1: Power down
3	RG_DRV_32K_CK_PDN	**Powers down DRV_32K_CK** 0: Power on 1: Power down
2	RG_G_DRV_2M_CK_PDN	**Powers down G_DRV_2M_CK** 0: Power on 1: Power down
1	RG_G_SMPS_AUD_CK_PDN	**Powers down G_SMPS_AUD_CK** 0: Power on 1: Power down
0	RG_G_SMPS_PD_CK_PDN	**Powers down G_SMPS_PD_CK** 0: Power on 1: Power down

023C **TOP_CKPDN_CON0_SET** **TOP_CKPDN_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TOP_CKPDN_CON0_SET	**Sets up TOP_CKPDN_CON0** 1'b0: Does not set 1'b1: Set

023E **TOP_CKPDN_CON0_CLR** **TOP_CKPDN_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON0_CLR	**Clears TOP_CKPDN_CON0** 1'b0: Does not clear 1'b1: Clear

0240 **TOP_CKPDN_CON1** **TOP_CKPDN control Register 1** **04A0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_PWMOC_AUD_6M_CK_PDN	RG_PWMOC_6M_CK_PDN	RG_AUXADC_CK_PDN	RG_BUCK_1M_CK_PDN	RG_STB_1M_CK_PDN	RG_FQMTR_CK_PDN	RG_RTC_2SEC_OFF_DET_PDN	RG_RTC32K_1V8_1_0_PDN	RG_RTC32K_1V8_0_0_PDN	RG_RTCDET_CK_PDN	RG_RTC_75K_CK_PDN	RG_RTC_MCLK_PDN	RG_RTC_32K_CK_PDN
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	1	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
12	RG_PWMOC_AUD_6M_CK_PDN	**Powers down PWMOC_AUD_6M_CK** 0: Power on 1: Power down
11	RG_PWMOC_6M_CK_PDN	**Powers down PWMOC_6M_CK** 0: Power on 1: Power down
10	RG_AUXADC_CK_PDN	**Powers down AUXADC_CK** 0: Power on 1: Power down
9	RG_BUCK_1M_CK_PDN	**Powers down BUCK_1M_CK** 0: Power on 1: Power down
8	RG_STB_1M_CK_PDN	**Powers down STB_1M_CK** 0: Power on 1: Power down
7	RG_FQMTR_CK_PDN	**Powers down FQMTR_CK** 0: Power on 1: Power down

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Bit(s)	Name	Description
6	RG_RTC_2SEC_OFF_DET_PDN	**Powers down RTC_2SEC_OFF_DET** 0: Power on 1: Power down
5	RG_RTC32K_1V8_1_O_PDN	**Powers down RTC32K_1V8_1_O** 0: Power on 1: Power down
4	RG_RTC32K_1V8_0_O_PDN	**Powers down RTC32K_1V8_0_O** 0: Power on 1: Power down
3	RG_RTCDET_CK_PDN	**Powers down RTCDET_CK** 0: Power on 1: Power down
2	RG_RTC_75K_CK_PDN	**Powers down RTC_75K_CK** 0: Power on 1: Power down
1	RG_RTC_MCLK_PDN	**Powers down RTC_MCLK** 0: Power on 1: Power down
0	RG_RTC_32K_CK_PDN	**Powers down RTC_32K_CK** 0: Power on 1: Power down

0242 **TOP_CKPDN_CON1_SET** **TOP_CKPDN_CON1 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON1_SET	**Sets up TOP_CKPDN_CON1** 1'b0: Does not set 1'b1: Set

0244 **TOP_CKPDN_CON1_CLR** **TOP_CKPDN_CON1 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON1_CLR	**Clears TOP_CKPDN_CON1** 1'b0: Does not clear 1'b1: Clear

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0246	TOP_CKPDN_CON2	TOP_CKPDN control Register 2	167C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_STRUP_LBAT_SEL_CK_PDN	RG_TRIM_75K_CK_PDN	RG_RTC_EOSC32_CK_PDN	RG_RTC_26M_CK_PDN	RG_INTRP_CK_PDN	RG_FQMTR_32K_CK_PDN	RG_ACCDET_CK_PDN		RG_PCHR_32K_CK_PDN	RG_BIF_X1_CK_PDN	RG_BIF_X4_CK_PDN	RG_BIF_X72_CK_PDN	RG_FGADC_DIG_CK_PDN	RG_FGADC_ANA_CK_PDN		
Type	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW		
Reset	0	0	0	1	0	1	1		0	1	1	1	1	1		

Bit(s)	Name	Description
15	RG_STRUP_LBAT_SEL_CK_PDN	**Powers down STRUP_LBAT_SEL_CK** 0: Power on 1: Power down
14	RG_TRIM_75K_CK_PDN	**Powers down TRIM_75K_CK** 0: Power on 1: Power down
13	RG_RTC_EOSC32_CK_PDN	**Powers down RTC_EOSC32_CK** 0: Power on 1: Power down
12	RG_RTC_26M_CK_PDN	**Powers down RTC_26M_CK** 0: Power on 1: Power down
11	RG_INTRP_CK_PDN	**Powers down INTRP_CK** 0: Power on 1: Power down
10	RG_FQMTR_32K_CK_PDN	**Powers down FQMTR_32K_CK** 0: Power on 1: Power down
9	RG_ACCDET_CK_PDN	**Powers down ACCDET_CK** 0: Power on 1: Power down
7	RG_PCHR_32K_CK_PDN	**Powers down PCHR_32K_CK** 0: Power on 1: Power down
6	RG_BIF_X1_CK_PDN	**Powers down BIF_X1_CK** 0: Power on 1: Power down
5	RG_BIF_X4_CK_PDN	**Powers down BIF_X4_CK** 0: Power on 1: Power down
4	RG_BIF_X72_CK_PDN	**Powers down BIF_X72_CK** 0: Power on 1: Power down
3	RG_FGADC_DIG_CK_PDN	**Powers down FGADC_DIG_CK** 0: Power on 1: Power down
2	RG_FGADC_ANA_CK_PDN	**Powers down FGADC_ANA_CK** 0: Power on 1: Power down

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0248 TOP_CKPDN_CON2_SET TOP_CKPDN_CON2 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON2_SET	**Sets up TOP_CKPDN_CON2** 1'b0: Does not set 1'b1: Set

024A TOP_CKPDN_CON2_CLR TOP_CKPDN_CON2 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON2_CLR	**Clears TOP_CKPDN_CON2** 1'b0: Does not clear 1'b1: Clear

024C TOP_CKPDN_CON3 TOP_CKPDN Control Register 3 0DE0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_G_SMPS_TEST_CK_PDN	RG_EOSC_CALI_TEST_CK_PDN	RG_BUCK_ANA_CK_PDN	RG_BUCK_32K_CK_PDN	RG_PCHR_TEST_CK_PDN	RG_FGADC_FT_CK_PDN	RG_BGR_TEST_CK_PDN	RG_SPI_CK_PDN	RG_SMPS_CK_DIV_PDN	RG_EFUSE_CK_PDN	RG_STRUP_32K_CK_PDN	RG_STRUP_75K_CK_PDN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1	1	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
11	RG_G_SMPS_TEST_CK_PDN	**Powers down G_SMPS_TEST_CK** 0: Power on 1: Power down
10	RG_EOSC_CALI_TEST_CK_PDN	**Powers down EOSC_CALI_TEST_CK** 0: Power on 1: Power down
9	RG_BUCK_ANA_CK_PDN	**Powers down BUCK_ANA_CK** 0: Power on 1: Power down
8	RG_BUCK_32K_CK_PDN	**Powers down BUCK_32K_CK** 0: Power on

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Bit(s)	Name	Description
		1: Power down
7	RG_PCHR_TEST_CK_PDN	**Powers down PCHR_TEST_CK** 0: Power on 1: Power down
6	RG_FGADC_FT_CK_PDN	**Powers down FGADC_FT_CK** 0: Power on 1: Power down
5	RG_BGR_TEST_CK_PDN	**Powers down BGR_TEST_CK** 0: Power on 1: Power down
4	RG_SPI_CK_PDN	**Powers down SPI_CK** 0: Power on 1: Power down
3	RG_SMPS_CK_DIV_PDN	**Powers down SMPS_CK_DIV** 0: Power on 1: Power down
2	RG_EFUSE_CK_PDN	**Powers down EFUSE_CK** 0: Power on 1: Power down
1	RG_STRUP_32K_CK_PDN	**Powers down STRUP_32K_CK** 0: Power on 1: Power down
0	RG_STRUP_75K_CK_PDN	**Powers down STRUP_75K_CK** 0: Power on 1: Power down

024E **TOP_CKPDN_CON3_SET** **TOP_CKPDN_CON3 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON3_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON3_SET	**Sets up TOP_CKPDN_CON3** 1'b0: Does not set 1'b1: Set

0250 **TOP_CKPDN_CON3_CLR** **TOP_CKPDN_CON3 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON3_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON3_	**Clears TOP_CKPDN_CON3**

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Bit(s)	Name	Description
	CLR	1'b0: Does not clear 1'b1: Clear

0252 **TOP_CKPDN_CON4** **TOP_CKPDN Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VGPU_9M_CK_PDN	RG_BUCK_VCORE_9M_CK_PDN		RG_BUCK_VMODEM_9M_CK_PDN	RG_BUCK_VPA_9M_CK_PDN	RG_BUCK_VSRAM_PROC_9M_CK_PDN	RG_BUCK_9M_CK_PDN
Type										RW	RW		RW	RW	RW	RW
Reset										0	0		0	0	0	0

Bit(s)	Name	Description
6	RG_BUCK_VGPU_9M_CK_PDN	**Powers down BUCK_VGPU_9M_CK** 0: Power on 1: Power down
5	RG_BUCK_VCORE_9M_CK_PDN	**Powers down BUCK_VCORE_9M_CK** 0: Power on 1: Power down
3	RG_BUCK_VMODEM_9M_CK_PDN	**Powers down BUCK_VMODEM_9M_CK** 0: Power on 1: Power down
2	RG_BUCK_VPA_9M_CK_PDN	**Powers down BUCK_VPA_9M_CK** 0: Power on 1: Power down
1	RG_BUCK_VSRAM_PROC_9M_CK_PDN	**Powers down BUCK_VSRAM_PROC_9M_CK** 0: Power on 1: Power down
0	RG_BUCK_9M_CK_PDN	**Powers down BUCK_9M_CK** 0: Power on 1: Power down

0254 **TOP_CKPDN_CON4_SET** **TOP_CKPDN_CON4 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON4_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON4_SET	**Sets up TOP_CKPDN_CON4** 1'b0: Does not set 1'b1: Set

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0256 **TOP_CKPDN_CON4_CLR** **TOP_CKPDN_CON4 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON4_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON4_CLR	**Clears TOP_CKPDN_CON4** 1'b0: Does not clear 1'b1: Clear

0258 **TOP_CKPDN_CON5** **TOP_CKPDN Control Register 5** **1FC0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_BUCK_AUD_1M_CK_PDN	RG_DRV_CHRIND_CK_PDN	RG_DRV_ISINK7_CK_PDN	RG_DRV_ISINK6_CK_PDN	RG_DRV_ISINK5_CK_PDN	RG_DRV_ISINK4_CK_PDN	RG_AUD18M_CK_PDN	RG_VOW12M_CK_PDN	RG_VOW32K_CK_PDN	RG_BUCK_VSRAM_MD_9M_CK_PDN	RG_BUCK_VMD1_9M_CK_PDN	RG_BUCK_VS1_9M_CK_PDN	RG_BUCK_VS2_9M_CK_PDN	RG_INTRP_PRE_OC_CK_PDN	RG_LDO_CALI_75K_CK_PDN
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	1	1	1	1	1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_BUCK_AUD_1M_CK_PDN	**Powers down BUCK_AUD_1M_CK** 0: Power on 1: Power down
13	RG_DRV_CHRIND_CK_PDN	**Powers down DRV_CHRIND_CK** 0: Power on 1: Power down
12	RG_DRV_ISINK7_CK_PDN	**Powers down DRV_ISINK7_CK** 0: Power on 1: Power down
11	RG_DRV_ISINK6_CK_PDN	**Powers down DRV_ISINK6_CK** 0: Power on 1: Power down
10	RG_DRV_ISINK5_CK_PDN	**Powers down DRV_ISINK5_CK** 0: Power on 1: Power down
9	RG_DRV_ISINK4_CK_PDN	**Powers down DRV_ISINK4_CK** 0: Power on 1: Power down
8	RG_AUD18M_CK_PDN	**Powers down AUD18M_CK** 0: Power on 1: Power down
7	RG_VOW12M_CK_PDN	**Powers down VOW12M_CK** 0: Power on

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Bit(s)	Name	Description
		1: Power down
6	RG_VOW32K_CK_PDN	**Powers down VOW32K_CK** 0: Power on 1: Power down
5	RG_BUCK_VSRAM_MD_9M_CK_PDN	**Powers down BUCK_VSRAM_MD_9M_CK** 0: Power on 1: Power down
4	RG_BUCK_VMD1_9M_CK_PDN	**Powers down BUCK_VMD1_9M_CK** 0: Power on 1: Power down
3	RG_BUCK_VS1_9M_CK_PDN	**Powers down BUCK_VS1_9M_CK** 0: Power on 1: Power down
2	RG_BUCK_VS2_9M_CK_PDN	**Powers down BUCK_VS2_9M_CK** 0: Power on 1: Power down
1	RG_INTRP_PRE_OC_CK_PDN	**Powers down INTRP_PRE_OC_CK** 0: Power on 1: Power down
0	RG_LDO_CALI_75K_CK_PDN	**Powers down LDO_CALI_75K_CK** 0: Power on 1: Power down

025A **TOP_CKPDN_CON5_SET** **TOP_CKPDN_CON5 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON5_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON5_SET	**Sets up TOP_CKPDN_CON5** 1'b0: Does not set 1'b1: Set

025C **TOP_CKPDN_CON5_CLR** **TOP_CKPDN_CON5 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON5_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON5_CLR	**Clears TOP_CKPDN_CON5** 1'b0: Does not clear 1'b1: Clear

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025E	TOP_CKSEL_CON0	TOP_CKSEL Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SRCLKEN_SRC_SEL		RG_OSC_SEL_HW_SRC_SEL			RG_AUXADC_CKSEL	RG_75K_32K_SEL	RG_FQMTR_CK_CKSEL			RG_DRV_ISINK3_CK_CKSEL	RG_DRV_ISINK2_CK_CKSEL	RG_DRV_ISINK1_CK_CKSEL	RG_DRV_ISINK0_CK_CKSEL	RG_AUD_CK_SEL	RG_AUDIF_CK_CKSEL
Type	RW		RW			RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_SRCLKEN_SRC_SEL	**Selects srclken source** 2'b00: From srclken0 2'b01: From srclken1 2'b10: From srclken0 and srclken1 2'b11: Reserved
13:12	RG_OSC_SEL_HW_SRC_SEL	**Selects OSC_SEL source under hardware control** 2'b00: From buck controller 2'b01: From srclken 2'b10: Reserved 2'b11: Reserved
10	RG_AUXADC_CK_CKSEL	**Selects AUXADC_CK clock** 1'b0: R_SMPS_CK/n 1'b1: R_AUD26_CK/n
9	RG_75K_32K_SEL	**Selects RTC_32K1V8_CK clock** 1'b0: R_PMU75K_CK/2 1'b1: R_RTC32K_CK
8:6	RG_FQMTR_CK_CKSEL	**Selects FQMTR_CK clock** 3'b000: R_AUD_26M_CK 3'b001: R_XOSC32_CK_DETECTION 3'b010: R_EOSC32_CK 3'b011: R_RTC32K_CK 3'b100: R_SMPS_CK 3'b101: R_RTC_TICK_SEC 3'b11x: R_PMU75K_CK
5	RG_DRV_ISINK3_CK_CKSEL	**Selects DRV_ISINK3_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
4	RG_DRV_ISINK2_CK_CKSEL	**Selects DRV_ISINK2_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
3	RG_DRV_ISINK1_CK_CKSEL	**Selects DRV_ISINK1_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
2	RG_DRV_ISINK0_CK_CKSEL	**Selects DRV_ISINK0_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
1	RG_AUD_CK_CKSEL	**Selects AUD_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_PAD_AUDIF_CK
0	RG_AUDIF_CK_CKS	**Selects AUDIF_CK clock**

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Bit(s)	Name	Description
	EL	1'b0: R_PAD_AUDIF_CK 1'b1: R_AUD_26M_CK

0260 **TOP_CKSEL_CON0_SET** **TOP_CKSEL_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON_SET	**Sets up TOP_CKSEL_CON0** 1'b0: Does not set 1'b1: Set

0262 **TOP_CKSEL_CON0_CLR** **TOP_CKSEL_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON_CLR	**Clears TOP_CKSEL_CON0** 1'b0: Does not clear 1'b1: Clear

0264 **TOP_CKSEL_CON1** **TOP_CKSEL Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DRV_CHRIND_CK_CKSEL	RG_DRV_ISINK7_CK_CKSEL	RG_DRV_ISINK6_CK_CKSEL	RG_DRV_ISINK5_CK_CKSEL	RG_DRV_ISINK4_CK_CKSEL	RG_FGADC_ANA_CK_CKSEL	RG_PCHR_TEST_CK_CKSEL	RG_BGR_TEST_CK_CKSEL	RG_STRUP_75K_CK_CKSEL	
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	RG_DRV_CHRIND_CK_CKSEL	**Selects DRV_CHRIND_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
8	RG_DRV_ISINK7_CK_CKSEL	**Selects DRV_ISINK7_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK

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Bit(s)	Name	Description
7	RG_DRV_ISINK6_CK_CKSEL	**Selects DRV_ISINK6_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
6	RG_DRV_ISINK5_CK_CKSEL	**Selects DRV_ISINK5_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
5	RG_DRV_ISINK4_CK_CKSEL	**Selects DRV_ISINK4_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
4	RG_FGADC_ANA_CK_CKSEL	**Selects FGADC_ANA_CK clock** 1'b0: R_RTC32K_CK 1'b1: FGADC_FT_CK_DIV8
3	RG_PCHR_TEST_CK_CKSEL	**Selects PCHR_TEST_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_SMPS_CK
2	RG_BGR_TEST_CK_CKSEL	**Selects BGR_TEST_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_SMPS_CK
1:0	RG_STRUP_75K_CK_CKSEL	**Selects STRUP_75K_CK clock** 2'b00: R_PMU75K_CK 2'b01: R_AUD_26M_CK 2'b1x: R_SMPS_CK

0266 TOP_CKSEL_CON1_SET TOP_CKSEL_CON1 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON1_SET	**Sets up TOP_CKSEL_CON1** 1'b0: Does not set 1'b1: Set

0268 TOP_CKSEL_CON1_CLR TOP_CKSEL_CON1 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON1_CLR	**Clears TOP_CKSEL_CON1** 1'b0: Does not clear 1'b1: Clear

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026A TOP_CKSEL_CON2 TOP_CKSEL Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VOWEN_MODE	RG_BUCK_OSC_SEL_MODE		RG_SRCVOLTEN_MODE	RG_VOWEN_SW	RG_BUCK_OSC_SEL_SW		RG_SRCVOLTEN_SW
Type									RW	RW		RW	RW	RW		RW
Reset									0	0		0	0	0		0

Bit(s)	Name	Description
7	RG_VOWEN_MODE	**VOWEN mode** 1'b0: HW mode 1'b1: SW mode
6	RG_BUCK_OSC_SEL_MODE	**BUCK_OSC_SEL mode** 1'b0: HW mode 1'b1: SW mode
4	RG_SRCVOLTEN_MODE	**SRCVOLTEN mode** 1'b0: HW mode 1'b1: SW mode
3	RG_VOWEN_SW	**VOWEN SW mode value**
2	RG_BUCK_OSC_SEL_SW	**BUCK_OSC_SEL SW mode value**
0	RG_SRCVOLTEN_SW	**SRCVOLTEN SW mode value**

026C TOP_CKSEL_CON2_SET TOP_CKSEL_CON2 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON2_SET	**Sets up TOP_CKSEL_CON2** 1'b0: Does not set 1'b1: Set

026E TOP_CKSEL_CON2_CLR TOP_CKSEL_CON2 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	TOP_CKSEL_CON2_CLR	**Clears TOP_CKSEL_CON2** 1'b0: Does not clear 1'b1: Clear

0276 **TOP_CKDIVSEL_CON0** **TOP_CKDIVSEL Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON0_RSV						RG_REG_CK_DIVSEL			RG_BIF_X4_CK_DIVSEL					RG_STRUP_LBAT_SEL_CK_DIVSEL	
Type	RW						RW			RW					RW	
Reset	0	0	0	0	0	0	0	0		0	0	0			0	1

Bit(s)	Name	Description
15:10	TOP_CKDIVSEL_CON0_RSV	
9:8	RG_REG_CK_DIVSEL	**Selects REG_CK divider** 2'b00: DIV1 2'b01: DIV2 2'b10: DIV4 2'b11: DIV8
6:4	RG_BIF_X4_CK_DIVSEL	**Selects BIF_X4_CK divider** 3'b000: DIV1 3'b001: DIV2 3'b010: DIV4 3'b011: DIV8 3'b1xx: DIV16
1:0	RG_STRUP_LBAT_SEL_CK_DIVSEL	**Selects STRUP_LBAT_SEL_CK divider** 2'b00: DIV18 2'b01: DIV9 2'b10: DIV4 2'b11: DIV2

0278 **TOP_CKDIVSEL_CON0_SET** **TOP_CKDIVSEL_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON0_SET	**Sets up TOP_CKDIVSEL_CON0** 1'b0: Does not set 1'b1: Set

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027A **TOP_CKDIVSEL_CON0_CLR** **TOP_CKDIVSEL_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON0_CLR	**Clears TOP_CKDIVSEL_CON0** 1'b0: Does not clear 1'b1: Clear

027C **TOP_CKDIVSEL_CON1** **TOP_CKDIVSEL Control Register 1** **0015**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BUCK_9M_CK_DIVSEL	RG_AUXADC_26M_CK_DIVSEL		RG_AUXADC_SMPS_CK_DIVSEL	
Type												RW	RW		RW	
Reset												1	0	1	0	1

Bit(s)	Name	Description
4	RG_BUCK_9M_CK_DIVSEL	**Selects BUCK_9M_CK divider** 1'b0: DIV1 1'b1: DIV2
3:2	RG_AUXADC_26M_CK_DIVSEL	**Selects AUXADC_26M_CK divider** 2'b00: DIV26 2'b01: DIV13 2'b1x: DIV8
1:0	RG_AUXADC_SMPS_CK_DIVSEL	**Selects AUXADC_SMPS_CK divider** 2'b00: DIV18 2'b01: DIV9 2'b10: DIV6 2'b11: DIV4

027E **TOP_CKDIVSEL_CON1_SET** **TOP_CKDIVSEL_CON1 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON1_SET	**Sets up TOP_CKDIVSEL_CON1** 1'b0: Does not set 1'b1: Set

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0280 **TOP_CKDIVSEL_CON1_CLR** **TOP_CKDIVSEL_CON1 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON1_CLR	**Clears TOP_CKDIVSEL_CON1** 1'b0: Does not clear 1'b1: Clear

0282 **TOP_CKHWEN_CON0** **TOP_CKHWEN Control Register 0** **30FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUXADC_CK_CKSEL_HWEN	RG_AUXADC_26M_CK_PDN_HWEN			RG_RTC_26M_CK_PDN_HWEN	RG_EFUSE_CK_PDN_HWEN	RG_BUCK_1M_CK_PDN_HWEN	RG_AUXADC_SMPS_CK_PDN_HWEN	RG_AUXADC_CK_PDN_HWEN	RG_GDRV_2M_CK_PDN_HWEN	RG_SMPS_AUD_CK_PDN_HWEN	RG_SMPS_PD_CK_PDN_HWEN
Type					RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0			1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11	RG_AUXADC_CK_CKSEL_HWEN	**Controls AUXADC_CK clock selection** 0: SW mode 1: HW mode
10	RG_AUXADC_26M_CK_PDN_HWEN	**Controls AUXADC_26m_CK clock selection** 0: SW mode 1: HW mode
7	RG_RTC_26M_CK_PDN_HWEN	**Controls RTC_26M_CK power-down** 0: SW mode 1: HW mode
6	RG_EFUSE_CK_PDN_HWEN	**Controls EFUSE_CK power-down** 0: SW mode 1: HW mode
5	RG_BUCK_1M_CK_PDN_HWEN	**Controls BUCK_1M_CK power-down** 0: SW mode 1: HW mode
4	RG_AUXADC_SMPS_CK_PDN_HWEN	**Controls AUXADC_SMPS_CK power down** 0: SW mode 1: HW mode
3	RG_AUXADC_CK_PDN_HWEN	**Controls AUXADC_CK power-down** 0: SW mode 1: HW mode

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Bit(s)	Name	Description
2	RG_G_DRV_2M_CK_PDN_HWEN	**Controls G_DRV_2M_CK power-down** 0: SW mode 1: HW mode
1	RG_G_SMPS_AUD_CK_PDN_HWEN	**Controls G_SMPS_AUD_CK power-down** 0: SW mode 1: HW mode
0	RG_G_SMPS_PD_CK_PDN_HWEN	**Controls G_SMPS_PD_CK power-down** 0: SW mode 1: HW mode

0284 TOP_CKHWEN_CON0_SET TOP_CKHWEN_CON0 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON0_SET	**Sets up TOP_CKHWEN_CON0** 1'b0: Does not set 1'b1: Set

0286 TOP_CKHWEN_CON0_CLR TOP_CKHWEN_CON0 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON0_CLR	**Clears TOP_CKHWEN_CON0** 1'b0: Does not clear 1'b1: Clear

0288 TOP_CKHWEN_CON1 TOP_CKHWEN Control Register 1 3037

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BUCK_VGPU_9M_CK_PDN_HWEN	RG_BUCK_VCORE_9M_CK_PDN_HWEN		RG_BUCK_VMODEM_9M_CK_PDN_HWEN	RG_BUCK_VPA_9M_CK_PDN_HWEN	RG_BUCK_VSRAM_PROC_9M_CK_PDN_HWEN
Type											RW	RW		RW	RW	RW

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Reset											1	1		1	1	1

Bit(s)	Name	Description
5	RG_BUCK_VGPU_9M_CK_PDN_HWEN	**Controls BUCK_VGPU_9M_CK power-down** 0: SW mode 1: HW mode
4	RG_BUCK_VCORE_9M_CK_PDN_HWEN	**Controls BUCK_VCORE_9M_CK power-down** 0: SW mode 1: HW mode
2	RG_BUCK_VMODEM_9M_CK_PDN_HWEN	**Controls BUCK_VMODEM_9M_CK power-down** 0: SW mode 1: HW mode
1	RG_BUCK_VPA_9M_CK_PDN_HWEN	**Controls BUCK_VPA_9M_CK power-down** 0: SW mode 1: HW mode
0	RG_BUCK_VSRAM_PROC_9M_CK_PDN_HWEN	**Controls BUCK_VSRAM_PROC_9M_CK power-down** 0: SW mode 1: HW mode

028A TOP_CKHWEN_CON1_SET TOP_CKHWEN_CON1 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON1_SET	**Sets up TOP_CKHWEN_CON1** 1'b0: Does not set 1'b1: Set

028C TOP_CKHWEN_CON1_CLR TOP_CKHWEN_CON1 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON1_CLR	**Clears TOP_CKHWEN_CON1** 1'b0: Does not clear 1'b1: Clear

028E TOP_CKHWEN_CON2 TOP_CKHWEN Control Register 2 002F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name											RG_BUCK_AUD_1M_CK_PDN_HWEN	RG_AUD18M_CK_PDN_HWEN	RG_BUCK_VSRAM_MD_9M_CK_PDN_HWEN	RG_BUCK_VMD1_9M_CK_PDN_HWEN	RG_BUCK_VS1_9M_CK_PDN_HWEN	RG_BUCK_VS2_9M_CK_PDN_HWEN
Type											RW	RW	RW	RW	RW	RW
Reset											1	0	1	1	1	1

Bit(s)	Name	Description
5	RG_BUCK_AUD_1M_CK_PDN_HWEN	**Controls BUCK_AUD_1M_CK power-down** 0: SW mode 1: HW mode
4	RG_AUD18M_CK_PDN_HWEN	**Controls AUD18M_CK power-down** 0: SW mode 1: HW mode
3	RG_BUCK_VSRAM_MD_9M_CK_PDN_HWEN	**Controls BUCK_VSRAM_MD_9M_CK power-down** 0: SW mode 1: HW mode
2	RG_BUCK_VMD1_9M_CK_PDN_HWEN	**Controls BUCK_VMD1_9M_CK power-down** 0: SW mode 1: HW mode
1	RG_BUCK_VS1_9M_CK_PDN_HWEN	**Controls BUCK_VS1_9M_CK power-down** 0: SW mode 1: HW mode
0	RG_BUCK_VS2_9M_CK_PDN_HWEN	**Controls BUCK_VS2_9M_CK power-down** 0: SW mode 1: HW mode

0290 TOP_CKHWEN_CON2_SET TOP_CKHWEN_CON2 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON2_SET	**Sets up TOP_CKHWEN_CON2** 1'b0: Does not set 1'b1: Set

0292 TOP_CKHWEN_CON2_CLR TOP_CKHWEN_CON2 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON2_CLR	**Clears TOP_CKHWEN_CON2** 1'b0: Does not clear 1'b1: Clear

029A **TOP_CLKSQ** **TOP_CLKSQ Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VA18				RG_CLKSQ_IN_SEL_VA18_SWCTRL	RG_CLKSQ_IN_SEL_VA18	RG_CLKSQ_EN_AUX_MD_MODE	RG_CLKSQ_EN_AUX_AP_MODE				RG_CLKSQ_EN_AUX_GPS	RG_CLKSQ_EN_AUX_MD	RG_CLKSQ_EN_AUX_AP	RG_CLKSQ_EN_FQR	RG_CLKSQ_EN_AUD
Type	RO				RW	RW	RW	RW				RW	RW	RW	RW	RW
Reset	0				0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VA18	**Status of CLKSQ** 0: Disable 1: Enable
11	RG_CLKSQ_IN_SEL_VA18_SWCTRL	**CLKSQ_IN_SEL_VA18 SW control** 0: HW control 1: SW control
10	RG_CLKSQ_IN_SEL_VA18	**Enables CLKSQ_IN_SEL_VA18 SW** 0: SW mode 1: HW mode: SRCLKEN_IN0
9	RG_CLKSQ_EN_AUX_MD_MODE	**Selects CLKSQ_EN_AUX_MD mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
8	RG_CLKSQ_EN_AUX_AP_MODE	**Selects CLKSQ_EN_AUX_AP mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
4	RG_CLKSQ_EN_AUX_GPS	**Enables CLKSQ for GPS** 0: Disable clock 1: Enable clock
3	RG_CLKSQ_EN_AUX_MD	**Enables CLKSQ for MD (SW mode)** 0: Disable clock 1: Enable clock
2	RG_CLKSQ_EN_AUX_AP	**Enables CLKSQ for AP (SW mode)** 0: Disable clock 1: Enable clock
1	RG_CLKSQ_EN_FQR	**Enables CLKSQ for FQMTR** 0: Disable clock 1: Enable clock
0	RG_CLKSQ_EN_AUD	**Enables CLKSQ for AUDIO** 0: Disable clock 1: Enable clock

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029C **TOP_CLKSQ_SET** **TOP_CLKSQ Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_SET	**Sets up TOP_CLKSQ** 1'b0: Does not set 1'b1: Set

029E **TOP_CLKSQ_CLR** **TOP_CLKSQ Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_CLR	**Clears TOP_CLKSQ** 1'b0: Does not clear 1'b1: Clear

02A0 **TOP_CLKSQ_RTC** **TOP_CLKSQ_RTC Register** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VDIG18														RG_CLKSQ_RTC_EN_HW_MODE	RG_CLKSQ_RTC_EN
Type	RO														RW	RW
Reset	0														1	0

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VDIG18	**Status of CLKSQ_RTC** 0: Disable 1: Enable
1	RG_CLKSQ_RTC_EN_HW_MODE	**CLKSQ_RTC HW mode** If enabled, CLKSQ_RTC will be from HW control. If disabled, CLKSQ_RTC will be from RG_CLKSQ_RTC_EN. 0: SW mode 1: HW mode
0	RG_CLKSQ_RTC_EN	**Enables CLKSQ_RTC** 0: Disable clock 1: Enable clock

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02A2 **TOP_CLKSQ_RTC_SET** **TOP_CLKSQ_RTC Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_RTC_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_SET	**Sets up TOP_CLKSQ_RTC** 1'b0: Does not set 1'b1: Set

02A4 **TOP_CLKSQ_RTC_CLR** **TOP_CLKSQ_RTC Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_RTC_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_CLR	**Clears TOP_CLKSQ_RTC** 1'b0: Does not clear 1'b1: Clear

02A6 **TOP_CLK_TRIM** **TOP_CLK_TRIM Register** **0C6C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DA_OSC_75K_TRIM												
Type				RO												
Reset				0	1	1	0	0								

Bit(s)	Name	Description
12:8	DA_OSC_75K_TRIM	75kHz OSC trimming bit

02B6 **TOP_RST_MISC** **Reset Control Misc** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_PWRKEY_RST_EN	RG_HOMEKEY_RST_EN							RG_WDTRSTB_MODE	
Type							RW	RW							RW	
Reset							1	0							0	

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Bit(s)	Name	Description
9	RG_PWRKEY_RST_EN	**Enables PWRKEY long press reset** 1'b1: Enable reset 1'b0: Disable reset
8	RG_HOMEKEY_RST_EN	**Enables HOMEKEY long press reset** 1'b1: Enable reset 1'b0: Disable reset
1	RG_WDTRSTB_MODE	**Selects WDTRSTB reset state** 1'b0: State 0; no re-power on and reset digital only 1'b1: State 1; re-power on

041E **BUCK_OC_CON0** **BUCK_OC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUCK_VPA_OC_STATUS	BUCK_VS2_OC_STATUS	BUCK_VS1_OC_STATUS	BUCK_VSRAM_MD_OC_STATUS	BUCK_VMD1_OC_STATUS	BUCK_VMODEM_OC_STATUS	BUCK_VGPU_OC_STATUS	BUCK_VCORE_OC_STATUS
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	BUCK_VPA_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
6	BUCK_VS2_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
5	BUCK_VS1_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
4	BUCK_VSRAM_MD_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
3	BUCK_VMD1_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
2	BUCK_VMODEM_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
1	BUCK_VGPU_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
0	BUCK_VCORE_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.

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0424 BUCK_OC_CON3 BUCK_OC Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUCK_VPA_OC_FLAG_CLR	BUCK_VS2_OC_FLAG_CLR	BUCK_VS1_OC_FLAG_CLR	BUCK_VSRAM_MD_OC_FLAG_CLR	BUCK_VMD1_OC_FLAG_CLR	BUCK_VMODEM_OC_FLAG_CLR	BUCK_VGPU_OC_FLAG_CLR	BUCK_VCORE_OC_FLAG_CLR
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	BUCK_VPA_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
6	BUCK_VS2_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
5	BUCK_VS1_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
4	BUCK_VSRAM_MD_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
3	BUCK_VMD1_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
2	BUCK_VMODEM_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
1	BUCK_VGPU_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status
0	BUCK_VCORE_OC_FLAG_CLR	0: Keep OC status 1: Clear OC status

0426 BUCK_OC_CON4 BUCK_OC Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUCK_VPA_OC_FLAG_CLR_SEL	BUCK_VS2_OC_FLAG_CLR_SEL	BUCK_VS1_OC_FLAG_CLR_SEL	BUCK_VSRAM_MD_OC_FLAG_CLR_SEL	BUCK_VMD1_OC_FLAG_CLR_SEL	BUCK_VMODEM_OC_FLAG_CLR_SEL	BUCK_VGPU_OC_FLAG_CLR_SEL	BUCK_VCORE_OC_FLAG_CLR_SEL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	BUCK_VPA_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
6	BUCK_VS2_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.

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Bit(s)	Name	Description
5	BUCK_VS1_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
4	BUCK_VSRAM_MD_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
3	BUCK_VMD1_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
2	BUCK_VMODEM_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
1	BUCK_VGPU_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.
0	BUCK_VCORE_OC_FLAG_CLR_SEL	0: HW clears OC status. 1: SW clears OC status.

0438 **SMPS_ANA_CON0** **SMPS Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VPA_BURSTL		RG_VPA_BURSTH													
Type	RW		RW													
Reset	0	0	0	0												

Bit(s)	Name	Description
15:14	RG_VPA_BURSTL	**PWM/BURST threshold** 00: VH=0.35V (default) 01: VH=0.30V 10: VH=0.25V 11: VH=0.45V
13:12	RG_VPA_BURSTH	**PWM/BURST threshold** 00: VH=0.50V (default) 01: VH=0.45V 10: VH=0.35V 11: VH=0.60V

044C **SMPS_ANA_CON10** **SMPS Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VOUTDET_EN								
Type								RW								
Reset								0								

Bit(s)	Name	Description
8	RG_VOUTDET_EN	**Enables VOUT tied to VBAT detection** 0: Disable 1: Enable

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044E **VCORE_ANA_CON0** **VCORE Control Register 0** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VCORE_MODESET	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VCORE_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

0460 **VCORE_ANA_CON9** **VCORE Control Register 9** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RGS_QI_VCORE_OC_STATUS									
Type							RO									
Reset							0									

Bit(s)	Name	Description
9	RGS_QI_VCORE_OC_STATUS	**OC status** H: OC L: Normal operation

0462 **VGPU_ANA_CON0** **VGPU Control Register 0** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VGPU_MODESET	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VGPU_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

0474 **VGPU_ANA_C** **VGPU Control Register 9** **0020**

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ON9

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RGS_QI_VGPU_OC_STATUS									
Type							RO									
Reset							0									

Bit(s)	Name	Description
9	RGS_QI_VGPU_OC_STATUS	**OC status** H: OC L: Normal operation

0476 VSRAM_MD_ANA_CON0 VSRAM_MD Control Register 0 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VSRAM_MD_MODESET	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VSRAM_MD_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

0488 VSRAM_MD_ANA_CON9 VSRAM_MD Control Register 9 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RGS_QI_VSRAM_MD_OC_STATUS				
Type												RO				
Reset												0				

Bit(s)	Name	Description
4	RGS_QI_VSRAM_MD_OC_STATUS	**OC status** H: OC L: Normal operation

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048A VMODEM_ANA_CON0 VMODEM Control Register 0 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VMODEM_MODESET	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VMODEM_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

049C VMODEM_ANA_CON9 VMODEM Control Register 9 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RGS_QI_VMODEM_OC_STATUS				
Type												RO				
Reset												0				

Bit(s)	Name	Description
4	RGS_QI_VMODEM_OC_STATUS	**OC status** H: OC L: Normal operation

049E VMD1_ANA_CON0 VMD1 Control Register 0 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VMD1_MODESET	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VMD1_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

04B0 VMD1_ANA_C VMD1 Control Register 9 0001

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ON9

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RGS_QI_VMD1_OC_STATUS**				
Type												RO				
Reset												0				

Bit(s)	Name	Description
4	RGS_QI_VMD1_OC_STATUS	**OC status** H: OC L: Normal operation

04B2 **VS1_ANA_CON0** **VS1 Control Register 0** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_VS1_MODESET**	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VS1_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

04C4 **VS1_ANA_CON9** **VS1 Control Register 9** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RGS_QI_VS1_OC_STATUS**				
Type												RO				
Reset												0				

Bit(s)	Name	Description
4	RGS_QI_VS1_OC_STATUS	**OC status** H: OC L: Normal operation

04C6 **VS2_ANA_CON0** **VS2 Control Register 0** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															**RG_VS2_MODESET**	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	RG_VS2_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

04D8 VS2_ANA_CON9 VS2 Control Register 9 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RGS_QI_VS2_OC_STATUS**				
Type												RO				
Reset												0				

Bit(s)	Name	Description
4	RGS_QI_VS2_OC_STATUS	**OC status** H: OC L: Normal operation

04DA VPA_ANA_CON0 VPA Control Register 0 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RG_VPA_MODESET**			
Type													RW			
Reset													0			

Bit(s)	Name	Description
3	RG_VPA_MODESET	1'b1: Force PWM mode 1'b0: Auto mode

04E4 VPA_ANA_CON5 VPA Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RGS_QI_VPA_OC_STATUS**
Type																RO

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Reset																0

Bit(s)	Name	Description
0	RGS_QI_VPA_OC_STATUS	**Over-current status** 0: No over-current occurs. 1: Over-current occurs.

0608 BUCK_VCORE_CON4 BUCK_VCORE Control Register 4 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VCORE_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

060A BUCK_VCORE_CON5 BUCK_VCORE Control Register 5 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VCORE_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

061C BUCK_VGPU_CON4 BUCK_VGPU Control Register 4 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VGPU_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VGPU_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

061E BUCK_VGPU_CON5 BUCK_VGPU Control Register 5 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										BUCK_VGPU_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VGPU_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

0630 BUCK_VMODEM_CON4 BUCK_VMODEM Control Register 4 0030

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VMODEM_VOSEL						
Type										RW						
Reset										0	1	1	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VMODEM_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

0632 BUCK_VMODEM_CON5 BUCK_VMODEM Control Register 5 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VMODEM_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VMODEM_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

0644 BUCK_VMD1_CON4 BUCK_VMD1 Control Register 4 0030

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VMD1_VOSEL						
Type										RW						
Reset										0	1	1	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VMD1_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

0646 BUCK_VMD1_CON5 BUCK_VMD1 Control Register 5 0030

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VMD1_VOSEL_ON						
Type										RW						
Reset										0	1	1	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VMD1_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

0658 BUCK_VSRAM_MD_CON4 BUCK_VSRAM_MD Control Register 4 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VSRAM_MD_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VSRAM_MD_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

065A BUCK_VSRAM_MD_CON5 BUCK_VSRAM_MD Control Register 5 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VSRAM_MD_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VSRAM_MD_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

066C BUCK_VS1_CON4 BUCK_VS1 Control Register 4 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS1_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VS1_VOSEL	**Selects VOUT in SW mode** Voltage = (0.6 + 0.00625*code)*2

066E BUCK_VS1_C BUCK_VS1 Control Register 5 0040

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ON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS1_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VS1_VOSEL_ON	Selects in normal mode when VOSEL is configured in HW mode

0680 **BUCK_VS2_CON4** **BUCK_VS2 Control Register 4** **000C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS2_VOSEL						
Type										RW						
Reset										0	0	0	1	1	0	0

Bit(s)	Name	Description
6:0	BUCK_VS2_VOSEL	**Selects VOUT in SW mode** Voltage = (0.6 + 0.00625*code)*2

0682 **BUCK_VS2_CON5** **BUCK_VS2 Control Register 5** **000C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS2_VOSEL_ON						
Type										RW						
Reset										0	0	0	1	1	0	0

Bit(s)	Name	Description
6:0	BUCK_VS2_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

0690 **BUCK_VPA_CON2** **BUCK_VPA Control Register 2** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DA_QI_VPA_EN													BUCK_VPA_EN
Type			RO													RW
Reset			0													0

Bit(s)	Name	Description
13	DA_QI_VPA_EN	Enable signal
0	BUCK_VPA_EN	Enable control in SW mode

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0694 BUCK_VPA_CON4 BUCK_VPA Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BUCK_VPA_VOSEL					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	BUCK_VPA_VOSEL	**Selects VOUT in SW mode** Voltage = (0.16 + 0.016*code)*3.125

0696 BUCK_VPA_CON5 BUCK_VPA Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BUCK_VPA_VOSEL_ON					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	BUCK_VPA_VOSEL_ON	Selects VOUT in normal mode when VOSEL is configured in HW mode

06A8 BUCK_VSRAM_PROC_CON4 BUCK_VSRAM_PROC Control Register 4 0050

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VSRAM_PROC_VOSEL						
Type										RW						
Reset										1	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VSRAM_PROC_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6 + 0.00625*code

0800 ZCD_CON0 ZCD Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDZCDMUXSEL_VAUDP15				RG_AUDZCDTIMEOUTMODESEL	RG_AUDZCDGAINSTEPSIZE		RG_AUDZCDGAINSTEPTIME			RG_AUDZCDENABLE
Type						RW				RW	RW		RW			RW
Reset						0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
10:8	RG_AUDZCDMUXSEL_VAUDP15	**Selects zero crossing detection mux** 000: Left line in & Right line in 001: Headphone L & headphone R 010: Handset 011: IV buffer 100: Bypass ZCD 101: Bypass ZCD 110: Bypass ZCD 111: Bypass ZCD
6	RG_AUDZCDTIMEOUTMODESEL	
5:4	RG_AUDZCDGAINSTEPSIZE	**Gain step size to change internal gain of ZCD** 00: 1dB 01: 2dB 10: 4dB 11: 8dB
3:1	RG_AUDZCDGAINSTEPTIME	**Gain step time to change internal gain of ZCD** 000: 0us 001: 250us 010: 500us 011: 1ms 100: 2s 101: 4ms 110: 8ms 111: 16ms
0	RG_AUDZCDENABLE	**Enables zero crossing detection (ZCD)** 0: Disable 1: Enable

0802 ZCD_CON1 ZCD Control Register 1 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDLOLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0804 ZCD_CON2 ZCD Control Register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

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Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDHPLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0806 ZCD_CON3 ZCD Control Register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0808 ZCD_CON4 ZCD Control Register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

080A ZCD_CON5 ZCD Control Register 5 3F3F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					

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Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	
5:0	RG_AUDINTGAIN1	

0810 ISINK0_CON0 ISINK0 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM0_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM0_FSEL	**Selects ISINK0 dimming frequency** Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

0812 ISINK0_CON1 ISINK0 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH0_STEP			ISINK_DIM0_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH0_STEP	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM0_DUTY	**ISINK ON-duty of dimming 0 control** N: (N+1)/32

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Bit(s)	Name	Description
		0: 1/32 1: 2/32 2: 3/32 31: 32/32

0814 ISINK0_CON2 ISINK0 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH0_TR1_SEL				ISINK_BREATH0_TR2_SEL				ISINK_BREATH0_TF1_SEL				ISINK_BREATH0_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH0_TR1_SEL	**Selects ISINK0 breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH0_TR2_SEL	**Selects ISINK0 breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH0_TF1_SEL	**Selects ISINK0 breath mode falling time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s

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Bit(s)	Name	Description
		8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TF2_SEL	**Selects ISINK0 breath mode falling time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

0816 ISINK0_CON3 ISINK0 Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH0_TON_SEL								ISINK_BREATH0_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH0_TON_SEL	**ISINK0 breath mode Ton time selection** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TOFF_SEL	**Selects ISINK0 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s

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Bit(s)	Name	Description
		4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0818 ISINK1_CON0 ISINK1 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM1_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM1_FSEL	**Selects ISINK1 dimming frequency** Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

081A ISINK1_CON1 ISINK1 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH1_STEP			ISINK_DIM1_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA

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Bit(s)	Name	Description
		110: 24mA 111: 24mA
11:7	ISINK_DIM1_DUTY	**ISINK ON-duty of dimming 1 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

081C ISINK1_CON2 ISINK1 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH1_TR1_SEL				ISINK_BREATH1_TR2_SEL				ISINK_BREATH1_TF1_SEL				ISINK_BREATH1_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH1_TR1_SEL	**Selects ISINK1 breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH1_TR2_SEL	**Selects ISINK1 breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH1_TF1_SEL	**Selects ISINK1 breath mode falling time for duty 0% ~ 30%** 0: 0.123s 1: 0.338s 2: 0.523s

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Bit(s)	Name	Description
		3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TF2_SEL	**Selects ISINK1 breath mode falling time for duty31% ~ 100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

081E **ISINK1_CON3** **ISINK1 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**ISINK_BREATH1_TON_SEL**								**ISINK_BREATH1_TOFF_SEL**			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH1_TON_SEL	**Selects ISINK1 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

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Bit(s)	Name	Description
3:0	ISINK_BREATH1_TOFF_SEL	**Selects ISINK1 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0820 ISINK4_CON0 ISINK4 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM4_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM4_FSEL	**Selects ISINK4 dimming frequency** (This register is set for SINK2 on chip.) Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

0822 ISINK4_CON1 ISINK4 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH4_STEP			ISINK_DIM4_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH4_STEP	**Coarse 6 step current level for ISINK CH4**

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Bit(s)	Name	Description
		(This register is set for SINK2 on chip.) 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM4_DUTY	**ISINK ON-duty of dimming 4 control** N: (N+1)/32 (This register is set for SINK2 on chip.) 0: 1/32 1: 2/32 2: 3/32 31: 32/32

0824 ISINK4_CON2 ISINK4 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH4_TR1_SEL				ISINK_BREATH4_TR2_SEL				ISINK_BREATH4_TF1_SEL				ISINK_BREATH4_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH4_TR1_SEL	**Selects ISINK4 breath mode rising time for duty 0%~30%** (This register is set for SINK2 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH4_TR2_SEL	**Selects ISINK4 breath mode rising time for duty 31%~100%** (This register is set for SINK2 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s

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Bit(s)	Name	Description
		11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH4_TF1_SEL	**Selects ISINK4 breath mode falling time for duty 0%~ 30%** (This register is set for SINK2 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH4_TF2_SEL	**Selects ISINK4 breath mode falling time for duty 31%~ 100%** (This register is set for SINK2 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

0826 ISINK4_CON3 ISINK4 Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH4_TON_SEL								ISINK_BREATH4_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH4_TON_SEL	**Selects ISINK4 breath mode Ton time** (This register is set for SINK2 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s

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Bit(s)	Name	Description
		4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH4_TOFF_SEL	**Selects ISINK4 breath mode Toff time** (This register is set for SINK2 on chip.) 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0828 ISINK5_CON0 ISINK5 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM5_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM5_FSEL	**Selects ISINK5 dimming frequency** (This register is set for SINK3 on chip.) Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

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082A ISINK5_CON1 ISINK5 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH5_STEP			ISINK_DIM5_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH5_STEP	**Coarse 6 step current level for ISINK CH5** (This register is set for SINK3 on chip.) 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM5_DUTY	**ISINK ON-duty of dimming 5 control** N: (N+1)/32 (This register is set for SINK3 on chip.) 0: 1/32 1: 2/32 2: 3/32 31: 32/32

082C ISINK5_CON2 ISINK5 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH5_TR1_SEL				ISINK_BREATH5_TR2_SEL				ISINK_BREATH5_TF1_SEL				ISINK_BREATH5_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH5_TR1_SEL	**Selects ISINK5 breath mode rising time for duty 0~30%** (This register is set for SINK3 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH5_TR	**Selects ISINK5 breath mode rising time for duty 31~100%**

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Bit(s)	Name	Description
	2_SEL	(This register is set for SINK3 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH5_TF1_SEL	**Selects ISINK5 breath mode falling time for duty 0~30%** (This register is set for SINK3 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH5_TF2_SEL	**Selects ISINK5 breath mode falling time for duty 31%~100%** (This register is set for SINK3 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

082E **ISINK5_CON3 ISINK5 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH5_TON_								ISINK_BREATH5_TOFF			

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					SEL								_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH5_TON_SEL	**Selects ISINK5 breath mode Ton time** (This register is set for SINK3 on chip.) 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH5_TOFF_SEL	**Selects ISINK5 breath mode Toff time** (This register is set for SINK3 on chip.) 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0834 ISINK_SFSTR ISINK Soft Start 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_SFSTR0_TC		ISINK_SFSTR0_EN		ISINK_SFSTR1_TC		ISINK_SFSTR1_EN		ISINK_SFSTR4_TC		ISINK_SFSTR4_EN		ISINK_SFSTR5_TC		ISINK_SFSTR5_EN
Type		RW		RW		RW		RW		RW		RW		RW		RW
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:13	ISINK_SFSTR0_TC	**Controls ISNIK0 soft start timing step** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us)

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Bit(s)	Name	Description
		2'b11: 4T (2us)
12	ISINK_SFSTR0_EN	**Controls ISINK0 soft start** 1'b1: Enable after starting the current step 1'b0: Disable
10:9	ISINK_SFSTR1_TC	**Controls ISINK1 soft start timing step** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
8	ISINK_SFSTR1_EN	**Controls ISINK1 soft start** 1'b1: Enable after starting the current step 1'b0: Disable
6:5	ISINK_SFSTR4_TC	**Controls ISINK2 soft start timing step** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
4	ISINK_SFSTR4_EN	**Controls ISINK2 soft start** 1'b1: Enable after starting the current step 1'b0: Disable
2:1	ISINK_SFSTR5_TC	**Controls ISINK3 soft start timing step** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
0	ISINK_SFSTR5_EN	**Controls ISINK3 soft start** 1'b1: Enable after starting the current step 1'b0: Disable

0836 <u>**ISINK_EN_CTRL**</u> **ISINK Enable Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_CH5_BIAS_EN	ISINK_CH4_BIAS_EN	ISINK_CH1_BIAS_EN	ISINK_CH0_BIAS_EN	ISINK_CHOP5_EN	ISINK_CHOP4_EN	ISINK_CHOP1_EN	ISINK_CHOP0_EN	ISINK_CH5_EN	ISINK_CH4_EN	ISINK_CH1_EN	ISINK_CH0_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	ISINK_CH5_BIAS_EN	**Enables ISINK Channel 5 bias CLK** (This register is set for SINK3 on chip.) 1'b0: Disable 1'b1: Enable
10	ISINK_CH4_BIAS_EN	**Enables ISINK Channel 4 CHOP CLK** (This register is set for SINK2 on chip.) 1'b0: Disable 1'b1: Enable

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Bit(s)	Name	Description
9	ISINK_CH1_BIAS_EN	**Enables ISINK Channel 1 CHOP CLK** 1'b0: Disable 1'b1: Enable
8	ISINK_CH0_BIAS_EN	**Enables ISINK Channel 0 CHOP CLK** 1'b0: Disable 1'b1: Enable
7	ISINK_CHOP5_EN	**Enables ISINK Channel 5 CHOP CLK** (This register is set for SINK3 on chip.) 1'b0: Disable 1'b1: Enable
6	ISINK_CHOP4_EN	**Enables ISINK Channel 4 CHOP CLK** (This register is set for SINK2 on chip.) 1'b0: Disable 1'b1: Enable
5	ISINK_CHOP1_EN	**Enables ISINK Channel 1 CHOP CLK** 1'b0: Disable 1'b1: Enable
4	ISINK_CHOP0_EN	**Enables ISINK Channel 0 CHOP CLK** 1'b0: Disable 1'b1: Enable
3	ISINK_CH5_EN	**Turns on ISINK Channel 5** (This register is set for SINK3 on chip.) 1'b0: Disable 1'b1: Enable
2	ISINK_CH4_EN	**Turns on ISINK Channel 4** (This register is set for SINK2 on chip.) 1'b0: Disable 1'b1: Enable
1	ISINK_CH1_EN	**Turns on ISINK Channel 1** 1'b0: Disable 1'b1: Enable
0	ISINK_CH0_EN	**Turns on ISINK Channel 0** 1'b0: Disable 1'b1: Enable

0838 **ISINK_MODE_CTRL** **ISINK Mode Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_CH0_MODE		ISINK_CH1_MODE		ISINK_CH4_MODE		ISINK_CH5_MODE									
Type	RW		RW		RW		RW									
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
15:14	ISINK_CH0_MODE	**Selects ISINK Channel 0 enable mode** 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
13:12	ISINK_CH1_MODE	**Selects ISINK Channel 1 enable mode**

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Bit(s)	Name	Description
		2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
11:10	ISINK_CH4_MODE	**Selects ISINK Channel 4 enable mode** (This register is set for SINK2 on chip.) 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
9:8	ISINK_CH5_MODE	**Selects ISINK Channel 5 enable mode** (This register is set for SINK3 on chip.) 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode

083A **ISINK_ANA_CON0** **ISINK Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DA_QI_B_ISINKS_CH1_STEP			DA_QI_B_ISINKS_CH0_STEP			DA_QI_A_ISINKS_CH1_STEP			DA_QI_A_ISINKS_CH0_STEP		
Type					RO			RO			RO			RO		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	DA_QI_B_ISINKS_CH1_STEP	**Coarse 6 step current level for ISINK CH5** (This register is set for SINK3 on chip.) 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
8:6	DA_QI_B_ISINKS_CH0_STEP	**Coarse 6 step current level for ISINK CH4** (This register is set for SINK2 on chip.) 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
5:3	DA_QI_A_ISINKS_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA

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Bit(s)	Name	Description
		111: 24mA
2:0	DA_QI_A_ISINKS_CH0_STEP	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA

084A CHRIND_CON0 CHRIND Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_DIM_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CHRIND_DIM_FSEL	**Selects CHRIND dimming frequency** Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

084C CHRIND_CON1 CHRIND Control Register 1 3000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CHRIND_STEP			CHRIND_DIM_DUTY											
Type		RW			RW											
Reset		0	1	1	0	0	0	0	0							

Bit(s)	Name	Description
14:12	CHRIND_STEP	**Coarse 6 step current level for CHRIND** 000: 2mA 001: 4mA 010: 4mA 011: 6mA 100: NA

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Bit(s)	Name	Description
		101: NA 110: NA 111: NA
11:7	CHRIND_DIM_DUTY	**ISINK ON-duty of dimming 0 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

084E **CHRIND_CON2** **CHRIND Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_BREATH_TR1_SEL				CHRIND_BREATH_TR2_SEL				CHRIND_BREATH_TF1_SEL				CHRIND_BREATH_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	CHRIND_BREATH_TR1_SEL	**Selects CHRIND breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	CHRIND_BREATH_TR2_SEL	**Selects CHRIND breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	CHRIND_BREATH_TF1_SEL	**Selects CHRIND breath mode falling time for duty 0%~30%** 0: 0.123s

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Bit(s)	Name	Description
		1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_TF2_SEL	**Selects CHRIND breath mode falling time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

0850 **CHRIND_CON3** **CHRIND Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CHRIND_BREATH_TON_SEL								CHRIND_BREATH_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	CHRIND_BREATH_TON_SEL	**Selects CHRIND breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s

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Bit(s)	Name	Description
		12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_TOFF_SEL	**Selects CHRIND breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0852 **CHRIND_EN_CTRL** **CHRIND Enable Control Simple** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CHRIND_BIAS_EN**		**CHRIND_MODE**		**CHRIND_CHOP_EN**	**CHRIND_EN**	**CHRIND_EN_SEL**	**CHRIND_SFSTR_TC**		**CHRIND_SFSTR_EN**
Type							RW		RW		RW	RW	RW	RW		RW
Reset							0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	CHRIND_BIAS_EN	**Enables CHRIND bias CLK** 1'b0: Disable 1'b1: Enable
7:6	CHRIND_MODE	**Selects CHRIND enable mode** 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
5	CHRIND_CHOP_EN	**Enables CHRIND CHOP CLK** 1'b0: Disable 1'b1: Enable
4	CHRIND_EN	**Turns on CHRIND** 1'b0: Disable 1'b1: Enable
3	CHRIND_EN_SEL	1'b0: Auto 1'b1: SW
2:1	CHRIND_SFSTR_TC	**Controls CHRIND soft start timing step** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us)

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Bit(s)	Name	Description
		2'b11: 4T (2us)
0	CHRIND_SFSTR_EN	**Controls CHRIND soft start** 1'b1: Enable after starting the current step 1'b0: Disable

0A00 **LDO_VA18_CON0** **LDO VA18 Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VA18_EN	DA_QI_VA18_STB						DA_QI_VA18_MODE					RG_VA18_ON_CTRL	RG_VA18_MODE_CTRL	RG_VA18_EN	RG_VA18_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VA18_EN	**VA18 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VA18_STB	
8	DA_QI_VA18_MODE	**VA18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VA18_ON_CTRL	**Controls VA18 enable** 1'b0: SW control by RG_VA18_EN 1'b1: HW control by SRCLKEN
2	RG_VA18_MODE_CTRL	**Controls VA18 low power mode** 1'b0: SW control by VA18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VA18_EN	**Enables VA18** 1'b1: Enable 1'b0: Disable
0	RG_VA18_MODE_SET	**VA18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A02 **LDO_VA18_CON1** **LDO VA18 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VA18_OCFB_EN	RG_VA18_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description

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Bit(s)	Name	Description
10	DA_QI_VA18_OCFB_EN	**VA18 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VA18_OCFB_EN	**Enables VA18 OCFB** 1'b1: Enable 1'b0: Disable

0A04 LDO_VTCXO24_CON0 LDO VTCXO24 Control Register 0 1A62

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VTCXO24_EN	DA_QI_VTCXO24_STB	RG_VTCXO24_SRCLK_EN_SEL					DA_QI_VTCXO24_MODE					RG_VTCXO24_ON_CTRL	RG_VTCXO24_MODE_CTRL	RG_VTCXO24_EN	RG_VTCXO24_MODE_SET
Type	RO	RO	RW					RO					RW	RW	RW	RW
Reset	0	0	0	1	1			0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VTCXO24_EN	**VTCXO24 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VTCXO24_STB	
13:11	RG_VTCXO24_SRCLK_EN_SEL	**Selects HW srclk enable** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN2 3'b011: SRCLKEN_IN0 or SRCLKEN_IN1 3'b100: SRCLKEN_IN0 or SRCLKEN_IN2 3'b101: SRCLKEN_IN1 or SRCLKEN_IN2 3'b110: SRCLKEN_IN0 and SRCLKEN_IN1 and SRCLKEN_IN2 3'b111: SRCLKEN_IN0 or SRCLKEN_IN1 or SRCLKEN_IN2
8	DA_QI_VTCXO24_MODE	**VTCXO24 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VTCXO24_ON_CTRL	**Controls VTCXO24 enable** 1'b0: SW control by RG_VTCXO24_EN 1'b1: HW control by SRCLKEN
2	RG_VTCXO24_MODE_CTRL	**Controls VTCXO24 low power mode** 1'b0: SW control by VTCXO24_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VTCXO24_EN	**Enables VTCXO24** 1'b1: Enable 1'b0: Disable
0	RG_VTCXO24_MODE_SET	**VTCXO24 low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A06 **LDO_VTCXO24_CON1** **LDO VTCXO24 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VTCXO24_OCFB_EN	RG_VTCXO24_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VTCXO24_OCFB_EN	**VTCXO24 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VTCXO24_OCFB_EN	**Enables VTCXO24 OCFB** 1'b1: Enable 1'b0: Disable

0A08 **LDO_VTCXO28_CON0** **LDO VTCXO28 Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VTCXO28_EN	DA_QI_VTCXO28_STB						DA_QI_VTCXO28_MODE					RG_VTCXO28_ON_CTRL	RG_VTCXO28_MODE_CTRL	RG_VTCXO28_EN	RG_VTCXO28_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VTCXO28_EN	**VTCXO28 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VTCXO28_STB	
8	DA_QI_VTCXO28_MODE	**VTCXO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VTCXO28_ON_CTRL	**Controls VTCXO28 enable** 1'b0: SW control by RG_VTCXO28_EN 1'b1: HW control by SRCLKEN
2	RG_VTCXO28_MODE_CTRL	**Controls VTCXO28 low power mode** 1'b0: SW control by VTCXO28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VTCXO28_EN	**Enables VTCXO28** 1'b1: Enable 1'b0: Disable
0	RG_VTCXO28_MODE_SET	**VTCXO28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A0A	LDO_VTCXO28_CON1	LDO VTCXO28 Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VTCXO28_OCFB_EN	RG_VTCXO28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VTCXO28_OCFB_EN	**VTCXO28 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VTCXO28_OCFB_EN	**Enables VTCXO28 OCFB** 1'b1: Enable 1'b0: Disable

0A0C	LDO_VCN28_CON0	LDO VCN28 Control Register 0	1A60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN28_EN	DA_QI_VCN28_STB						DA_QI_VCN28_MODE					RG_VCN28_ON_CTRL	RG_VCN28_MODE_CTRL	RG_VCN28_EN	RG_VCN28_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VCN28_EN	**VCN28 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VCN28_STB	
8	DA_QI_VCN28_MODE	**Selects VCN28 low power mode** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VCN28_ON_CTRL	**Controls VCN28 enable** 1'b0: SW control by RG_VCN28_EN 1'b1: HW control by SRCLKEN
2	RG_VCN28_MODE_CTRL	**Controls VCN28 low power mode** 1'b0: SW control by VCN28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCN28_EN	**Enables VCN28** 1'b1: Enable 1'b0: Disable
0	RG_VCN28_MODE_S	**VCN28 low power mode**

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Bit(s)	Name	Description
	ET	1'b0: Normal mode 1'b1: Low power mode

0A0E **LDO_VCN28_CON1** **LDO VCN28 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN28_OCFB_EN	RG_VCN28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN28_OCFB_EN	**VCN28 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCN28_OCFB_EN	**Enables VCN28 OCFB** 1'b1: Enable 1'b0: Disable

0A12 **LDO_VCAMA_CON0** **LDO VCAMA Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMA_EN	DA_QI_VCAMA_STB						DA_QI_VCAMA_MODE					RG_VCAMA_ON_CTRL		RG_VCAMA_EN	
Type	RO	RO						RO					RW		RW	
Reset	0	0						0					0		0	

Bit(s)	Name	Description
15	DA_QI_VCAMA_EN	**VCAMA enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VCAMA_STB	
8	DA_QI_VCAMA_MODE	**VCAMA low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VCAMA_ON_CTRL	**Controls VCAMA enable** 1'b0: SW control by RG_VCAMA_EN 1'b1: HW control by SRCLKEN
1	RG_VCAMA_EN	**Enables VCAMA** 1'b1: Enable 1'b0: Disable

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0A14 **LDO_VCAMA_CON1** **LDO VCAMA Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCAMA_OCFB_EN	RG_VCAMA_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMA_OCFB_EN	**VCAMA OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCAMA_OCFB_EN	**Enables VCAMA OCFB** 1'b1: Enable 1'b0: Disable

0A16 **LDO_VUSB33_CON0** **LDO VUSB33 Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VUSB33_EN	DA_QI_VUSB33_STB						DA_QI_VUSB33_MODE					RG_VUSB33_ON_CTRL	RG_VUSB33_MODE_CTRL	RG_VUSB33_EN	RG_VUSB33_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VUSB33_EN	**VUSB33 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VUSB33_STB	
8	DA_QI_VUSB33_MODE	**VUSB33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VUSB33_ON_CTRL	**Controls VUSB33 enable** 1'b0: SW control by RG_VUSB33_EN 1'b1: HW control by SRCLKEN
2	RG_VUSB33_MODE_CTRL	**Controls VUSB33 low power mode** 1'b0: SW control by VUSB33_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VUSB33_EN	**Enables VUSB33** 1'b1: Enable 1'b0: Disable
0	RG_VUSB33_MODE_SET	**VUSB33 low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A18 **LDO_VUSB33_CON1** **LDO VUSB33 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VUSB33_OCFB_EN	RG_VUSB33_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VUSB33_OCFB_EN	**VUSB33 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VUSB33_OCFB_EN	**Enables VUSB33 OCFB** 1'b1: Enable 1'b0: Disable

0A1C **LDO_VSIM1_CON0** **LDO VSIM1 Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM1_EN	DA_QI_VSIM1_STB						DA_QI_VSIM1_MODE					RG_VSIM1_ON_CTRL	RG_VSIM1_MODE_CTRL	RG_VSIM1_EN	RG_VSIM1_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VSIM1_EN	**VSIM1 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VSIM1_STB	
8	DA_QI_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSIM1_ON_CTRL	**Controls VSIM1 enable** 1'b0: SW control by RG_VSIM1_EN 1'b1: HW control by SRCLKEN
2	RG_VSIM1_MODE_CTRL	**Controls VSIM1 low power mode** 1'b0: SW control by VSIM1_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSIM1_EN	**VSIM1 enable** 1'b1: Enable 1'b0: Disable
0	RG_VSIM1_MODE_SET	**VSIM1 low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A1E **LDO_VSIM1_CON1** **LDO VSIM1 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VSIM1_OCFB_EN	RG_VSIM1_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VSIM1_OCFB_EN	**VSIM1 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VSIM1_OCFB_EN	**Enables VSIM1 OCFB** 1'b1: Enable 1'b0: Disable

0A22 **LDO_VSIM2_CON0** **LDO VSIM2 Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM2_EN	DA_QI_VSIM2_STB						DA_QI_VSIM2_MODE					RG_VSIM2_ON_CTRL	RG_VSIM2_MODE_CTRL	RG_VSIM2_EN	RG_VSIM2_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VSIM2_EN	**VSIM2 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VSIM2_STB	
8	DA_QI_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSIM2_ON_CTRL	**Controls VSIM2 enable** 1'b0: SW control by RG_VSIM2_EN 1'b1: HW control by SRCLKEN
2	RG_VSIM2_MODE_CTRL	**Controls VSIM2 low power mode** 1'b0: SW control by VSIM2_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSIM2_EN	**Enables VSIM2** 1'b1: Enable 1'b0: Disable
0	RG_VSIM2_MODE_SET	**VSIM2 low power mode** 1'b0: Normal mode

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Bit(s)	Name	Description
		1'b1: Low power mode

0A24 **LDO_VSIM2_CON1** **LDO VSIM2 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VSIM2_OCFB_EN	RG_VSIM2_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VSIM2_OCFB_EN	**VSIM2 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VSIM2_OCFB_EN	**Enables VSIM2 OCFB** 1'b1: Enable 1'b0: Disable

0A28 **LDO_VEMC_CON0** **LDO VEMC Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VEMC_EN	DA_QI_VEMC_STB						DA_QI_VEMC_MODE					RG_VEMC_ON_CTRL	RG_VEMC_MODE_CTRL	RG_VEMC_EN	RG_VEMC_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VEMC_EN	**VEMC enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VEMC_STB	
8	DA_QI_VEMC_MODE	**VEMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VEMC_ON_CTRL	**Controls VEMC enable** 1'b0: SW control by RG_VEMC_EN 1'b1: HW control by SRCLKEN
2	RG_VEMC_MODE_CTRL	**Controls VEMC low power mode** 1'b0: SW control by VEMC_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VEMC_EN	**Enables VEMC** 1'b1: Enable 1'b0: Disable

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Bit(s)	Name	Description
0	RG_VEMC_MODE_SET	**VEMC low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A2A **LDO_VEMC_CON1** **LDO VEMC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VEMC_OCFB_EN	RG_VEMC_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VEMC_OCFB_EN	**VEMC OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VEMC_OCFB_EN	**Enables VEMC OCFB** 1'b1: Enable 1'b0: Disable

0A2E **LDO_VMCH_CON0** **LDO VMCH Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMCH_EN	DA_QI_VMCH_STB						DA_QI_VMCH_MODE					RG_VMCH_ON_CTRL	RG_VMCH_MODE_CTRL	RG_VMCH_EN	RG_VMCH_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VMCH_EN	**VMCH enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VMCH_STB	
8	DA_QI_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VMCH_ON_CTRL	**Controls VMCH enable** 1'b0: SW control by RG_VMCH_EN 1'b1: HW control by SRCLKEN
2	RG_VMCH_MODE_CTRL	**Controls VMCH low power mode** 1'b0: SW control by VMCH_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VMCH_EN	**Enables VMCH**

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Bit(s)	Name	Description
		1'b1: Enable 1'b0: Disable
0	RG_VMCH_MODE_SET	**VMCH low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A30 **LDO_VMCH_CON1** **LDO VMCH Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VMCH_OCFB_EN	RG_VMCH_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VMCH_OCFB_EN	**VMCH OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VMCH_OCFB_EN	**Enables VMCH OCFB** 1'b1: Enable 1'b0: Disable

0A34 **LDO_VIO28_CON0** **LDO VIO28 Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO28_EN	DA_QI_VIO28_STB						DA_QI_VIO28_MODE					RG_VIO28_ON_CTRL	RG_VIO28_MODE_CTRL	RG_VIO28_EN	RG_VIO28_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VIO28_EN	**VIO28 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VIO28_STB	
8	DA_QI_VIO28_MODE	**VIO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VIO28_ON_CTRL	**Controls VIO28 enable** 1'b0: SW control by RG_VIO28_EN 1'b1: HW control by SRCLKEN
2	RG_VIO28_MODE_CTRL	**Controls VIO28 low power mode** 1'b0: SW control by VIO28_MODE_SET

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Bit(s)	Name	Description
		1'b1: HW control by SRCLKEN
1	RG_VIO28_EN	**Enables VIO28** 1'b1: Enable 1'b0: Disable
0	RG_VIO28_MODE_SET	**VIO28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A36 **LDO_VIO28_CON1** **LDO VIO28 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VIO28_OCFB_EN**	**RG_VIO28_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIO28_OCFB_EN	**VIO28 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VIO28_OCFB_EN	**Enables VIO28 OCFB** 1'b1: Enable 1'b0: Disable

0A3A **LDO_VIBR_CON0** **LDO VIBR Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VIBR_EN**	**DA_QI_VIBR_STB**						**DA_QI_VIBR_MODE**				**RG_VIBR_THER_SDN_EN**	**RG_VIBR_ON_CTRL**	**RG_VIBR_MODE_CTRL**	**RG_VIBR_EN**	**RG_VIBR_MODE_SET**
Type	RO	RO						RO				RW	RW	RW	RW	RW
Reset	0	0						0				0	0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VIBR_EN	**VIBR enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VIBR_STB	
8	DA_QI_VIBR_MODE	**VIBR low power mode status** 1'b0: Normal mode 1'b1: Low power mode
4	RG_VIBR_THER_SDN_EN	**Enables thermal shut-down** 1'b0: Disable 1'b1: Enable

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Bit(s)	Name	Description
3	RG_VIBR_ON_CTRL	**Controls VIBR enable** 1'b0: SW control by RG_VIBR_EN 1'b1: HW control by SRCLKEN
2	RG_VIBR_MODE_CTRL	**Controls VIBR low power mode** 1'b0: SW control by VIBR_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VIBR_EN	**Enables VIBR** 1'b1: Enable 1'b0: Disable
0	RG_VIBR_MODE_SET	**VIBR low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A3C **LDO_VIBR_CON1** **LDO VIBR Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VIBR_OCFB_EN**	**RG_VIBR_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIBR_OCFB_EN	**VIBR OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VIBR_OCFB_EN	**Enables VIBR OCFB** 1'b1: Enable 1'b0: Disable

0A40 **LDO_VCAMD_CON0** **LDO VCAMD Control Register 0** **0260**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VCAMD_EN**	**DA_QI_VCAMD_STB**						**DA_QI_VCAMD_MODE**						**RG_VCAMD_MODE_CTRL**	**RG_VCAMD_EN**	**RG_VCAMD_MODE_SET**
Type	RO	RO						RO						RW	RW	RW
Reset	0	0						0						0	0	0

Bit(s)	Name	Description
15	DA_QI_VCAMD_EN	**VCAMD enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VCAMD_STB	
8	DA_QI_VCAMD_MO	**VCAMD low power mode status**

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Bit(s)	Name	Description
	DE	1'b0: Normal mode 1'b1: Low power mode
2	RG_VCAMD_MODE_CTRL	**Controls VCAMD low power mode** 1'b0: SW control by VCAMD_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCAMD_EN	**Enables VCAMD** 1'b1: Enable 1'b0: Disable
0	RG_VCAMD_MODE_SET	**VCAMD low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A42 LDO_VCAMD_CON1 LDO VCAMD Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCAMD_OCFB_EN	RG_VCAMD_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMD_OCFB_EN	**VCAMD OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCAMD_OCFB_EN	**Enables VCAMD OCFB** 1'b1: Enable 1'b0: Disable

0A46 LDO_VRF18_CON0 LDO VRF18 Control Register 0 1A60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRF18_EN	DA_QI_VRF18_STB						DA_QI_VRF18_MODE					RG_VRF18_ON_CTRL	RG_VRF18_MODE_CTRL	RG_VRF18_EN	RG_VRF18_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VRF18_EN	**VRF18 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VRF18_STB	
8	DA_QI_VRF18_MODE	**VRF18 low power mode status** 1'b0: Normal mode

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Bit(s)	Name	Description
		1'b1: Low power mode
3	RG_VRF18_ON_CTRL	**Controls VRF18 enable** 1'b0: SW control by RG_VRF18_EN 1'b1: HW control by SRCLKEN
2	RG_VRF18_MODE_CTRL	**Controls VRF18 low power mode** 1'b0: SW control by VRF18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VRF18_EN	**Enables VRF18** 1'b1: Enable 1'b0: Disable
0	RG_VRF18_MODE_SET	**VRF18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A48 LDO_VRF18_CON1 LDO VRF18 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VRF18_OCFB_EN	RG_VRF18_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VRF18_OCFB_EN	**VRF18 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VRF18_OCFB_EN	**Enables VRF18 OCFB** 1'b1: Enable 1'b0: Disable

0A4C LDO_VIO18_CON0 LDO VIO18 Control Register 0 1A62

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO18_EN	DA_QI_VIO18_STB						DA_QI_VIO18_MODE					RG_VIO18_ON_CTRL	RG_VIO18_MODE_CTRL	RG_VIO18_EN	RG_VIO18_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VIO18_EN	**VIO18 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VIO18_STB	

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Bit(s)	Name	Description
8	DA_QI_VIO18_MODE	**VIO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VIO18_ON_CTRL	**Controls VIO18 enable** 1'b0: SW control by RG_VIO18_EN 1'b1: HW control by SRCLKEN
2	RG_VIO18_MODE_CTRL	**Controls VIO18 low power mode** 1'b0: SW control by VIO18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VIO18_EN	**Enables VIO18** 1'b1: Enable 1'b0: Disable
0	RG_VIO18_MODE_SET	**VIO18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A4E **LDO_VIO18_CON1** **LDO VIO18 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VIO18_OCFB_EN	RG_VIO18_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIO18_OCFB_EN	**VIO18 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VIO18_OCFB_EN	**Enables VIO18 OCFB** 1'b1: Enable 1'b0: Disable

0A52 **LDO_VCN18_CON0** **LDO VCN18 Control Register 0** **1A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN18_EN	DA_QI_VCN18_STB						DA_QI_VCN18_MODE					RG_VCN18_ON_CTRL	RG_VCN18_MODE_CTRL	RG_VCN18_EN	RG_VCN18_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VCN18_EN	**VCN18 enable status** 1'b1: Enable

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Bit(s)	Name	Description
		1'b0: Disable
14	DA_QI_VCN18_STB	
8	DA_QI_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VCN18_ON_CTRL	**Controls VCN18 enable** 1'b0: SW control by RG_VCN18_EN 1'b1: HW control by SRCLKEN
2	RG_VCN18_MODE_CTRL	**Controls VCN18 low power mode** 1'b0: SW control by VCN18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCN18_EN	**Enables VCN18** 1'b1: Enable 1'b0: Disable
0	RG_VCN18_MODE_SET	**VCN18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A54 **LDO_VCN18_CON1** **LDO VCN18 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN18_OCFB_EN	RG_VCN18_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN18_OCFB_EN	**VCN18 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCN18_OCFB_EN	**Enables VCN18 OCFB** 1'b1: Enable 1'b0: Disable

0A58 **LDO_VCAMIO_CON0** **LDO VCAMIO Control Register 0** **0260**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMIO_EN	DA_QI_VCAMIO_STB						DA_QI_VCAMIO_MODE						RG_VCAMIO_MODE_CTRL	RG_VCAMIO_EN	RG_VCAMIO_MODE_SET
Type	RO	RO						RO						RW	RW	RW
Reset	0	0						0						0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	DA_QI_VCAMIO_EN	**VCAMIO enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VCAMIO_STB	
8	DA_QI_VCAMIO_MODE	**VCAMIO low power mode** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCAMIO_MODE_CTRL	**Controls VCAMIO low power mode** 1'b0: SW control by VCAMIO_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCAMIO_EN	**Enables VCAMIO** 1'b1: Enable 1'b0: Disable
0	RG_VCAMIO_MODE_SET	**VCAMIO low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A5A **LDO_VCAMIO_CON1** **LDO VCAMIO Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VCAMIO_OCFB_EN**	**RG_VCAMIO_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMIO_OCFB_EN	**VCAMIO OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCAMIO_OCFB_EN	**Enables VCAMIO OCFB** 1'b1: Enable 1'b0: Disable

0A5E **LDO_VSRAM_PROC_CON0** **LDO VSRAM_PROC Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VSRAM_PROC_EN**	**DA_QI_VSRAM_PROC_STB**						**DA_QI_VSRAM_PROC_MODE**					**RG_VSRAM_PROC_ON_CTRL**	**RG_VSRAM_PROC_MODE_CTRL**	**RG_VSRAM_PROC_EN**	**RG_VSRAM_PROC_MODE_SET**
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

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Bit(s)	Name	Description
15	DA_QI_VSRAM_PROC_EN	**VSRAM_PROC enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VSRAM_PROC_STB	
8	DA_QI_VSRAM_PROC_MODE	**VSRAM_PROC low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSRAM_PROC_ON_CTRL	**Controls VSRAM_PROC enable** 1'b0: SW control by RG_VSRAM_PROC_EN 1'b1: HW control by SRCLKEN
2	RG_VSRAM_PROC_MODE_CTRL	**Controls VSRAM_PROC low power mode** 1'b0: SW control by VSRAM_PROC_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSRAM_PROC_EN	**Enables VSRAM_PROC** 1'b1: Enable 1'b0: Disable
0	RG_VSRAM_PROC_MODE_SET	**VSRAM_PROC low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A60 **LDO_VSRAM_PROC_CON1** **LDO VSRAM_PROC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VSRAM_PROC_OCFB_EN	RG_VSRAM_PROC_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VSRAM_PROC_OCFB_EN	**VSRAM_PROC OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VSRAM_PROC_OCFB_EN	**Enables VSRAM_PROC OCFB** 1'b1: Enable 1'b0: Disable

0A64 **LDO_VXO22_CON0** **LDO VXO22 Control Register 0** **1A62**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VXO22_EN	DA_QI_VXO22_STB						DA_QI_VXO22_MODE					RG_VXO22_ON_CTRL	RG_VXO22_MODE_CTRL	RG_VXO22_EN	RG_VXO22_MODE_SET

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Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VXO22_EN	**VXO22 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VXO22_STB	
8	DA_QI_VXO22_MODE	**VXO22 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VXO22_ON_CTRL	**Controls VXO22 enable** 1'b0: SW control by RG_VXO22_EN 1'b1: HW control by SRCLKEN
2	RG_VXO22_MODE_CTRL	**Controls VXO22 low power mode** 1'b0: SW control by VXO22_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VXO22_EN	**Enables VXO22** 1'b1: Enable 1'b0: Disable
0	RG_VXO22_MODE_SET	**VXO22 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A66 LDO_VXO22_CON1 LDO VXO22 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VXO22_OCFB_EN**	**RG_VXO22_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VXO22_OCFB_EN	**VXO22 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VXO22_OCFB_EN	**Enables VXO22 OCFB** 1'b1: Enable 1'b0: Disable

0A68 LDO_VRF12_CON0 LDO VRF12 Control Register 0 1A60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VRF12_EN**	**DA_QI_VRF12_STB**						**DA_QI_VRF12_MOD**					**RG_VRF12_ON_CTRL**	**RG_VRF12_MODE_C**	**RG_VRF12_EN**	**RG_VRF12_MODE_S**

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								E						TRL		ET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VRF12_EN	**VRF12 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VRF12_STB	
8	DA_QI_VRF12_MODE	**VRF12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VRF12_ON_CTRL	**Controls VRF12 enable** 1'b0: SW control by RG_VRF12_EN 1'b1: HW control by SRCLKEN
2	RG_VRF12_MODE_CTRL	**Controls VRF12 low power mode** 1'b0: SW control by VRF12_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VRF12_EN	**Enables VRF12** 1'b1: Enable 1'b0: Disable
0	RG_VRF12_MODE_SET	**VRF12 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A6A LDO_VRF12_CON1 LDO VRF12 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VRF12_OCFB_EN	RG_VRF12_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VRF12_OCFB_EN	**VRF12 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VRF12_OCFB_EN	**Enables VRF12 OCFB** 1'b1: Enable 1'b0: Disable

0A6E LDO_VA10_CON0 LDO VA10 Control Register 0 1A62

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VA10_E	DA_QI_VA10_ST						DA_QI_VA10_M					RG_VA10_ON_C	RG_VA10_MOD	RG_VA10_EN	RG_VA10_MOD

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	N	B						ODE					TRL	E_CT RL		E_SE T
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VA10_EN	**VA10 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VA10_STB	
8	DA_QI_VA10_MODE	**VA10 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VA10_ON_CTRL	**Controls VA10 enable** 1'b0: SW control by RG_VA10_EN 1'b1: HW control by SRCLKEN
2	RG_VA10_MODE_CTRL	**Controls VA10 low power mode** 1'b0: SW control by VA10_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VA10_EN	**Enables VA10** 1'b1: Enable 1'b0: Disable
0	RG_VA10_MODE_SET	**VA10 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A70 LDO_VA10_CON1 LDO VA10 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VA10_OCFB_EN	RG_VA10_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VA10_OCFB_EN	**VA10 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VA10_OCFB_EN	**Enables VA10 OCFB** 1'b1: Enable 1'b0: Disable

0A74 LDO_VDRAM_CON0 LDO VDRAM Control Register 0 1A62

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VD	DA_QI_VD						DA_QI_VD					RG_VDRA	RG_VDRA	RG_VDRA	RG_VDRA

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	RAM_EN	RAM_STB						RAM_MODE					M_ON_CTRL	M_MODE_CTRL	M_EN	M_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	1	0

Bit(s)	Name	Description
15	DA_QI_VDRAM_EN	**VDRAM enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VDRAM_STB	
8	DA_QI_VDRAM_MODE	**VDRAM low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VDRAM_ON_CTRL	**Controls VDRAM enable** 1'b0: SW control by RG_VDRAM_EN 1'b1: HW control by SRCLKEN
2	RG_VDRAM_MODE_CTRL	**Controls VDRAM low power mode** 1'b0: SW control by VDRAM_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VDRAM_EN	**Enables VDRAM** 1'b1: Enable 1'b0: Disable
0	RG_VDRAM_MODE_SET	**VDRAM low power mode** 1'b0: Normal mode 1'b1: L ow power mode

0A76 LDO_VDRAM_CON1 LDO VDRAM Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VDRAM_OCFB_EN	RG_VDRAM_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VDRAM_OCFB_EN	**VDRAM OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VDRAM_OCFB_EN	**Enables VDRAM OCFB** 1'b1: Enable 1'b0: Disable

0A7A LDO_VMIPI_CON0 LDO VMIPI Control Register 0 1A60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_Q	DA_Q						DA_Q					RG_V	RG_V	RG_V	RG_V

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	I_VMIPI_EN	I_VMIPI_STB						I_VMIPI_MODE					MIPI_ON_CTRL	MIPI_MODE_CTRL	MIPI_EN	MIPI_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VMIPI_EN	**VMIPI enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VMIPI_STB	
8	DA_QI_VMIPI_MODE	**VMIPI low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VMIPI_ON_CTRL	**Controls VMIPI enable** 1'b0: SW control by RG_VMIPI_EN 1'b1: HW control by SRCLKEN
2	RG_VMIPI_MODE_CTRL	**Controls VMIPI low power mode** 1'b0: SW control by VMIPI_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VMIPI_EN	**Enables VMIPI** 1'b1: Enable 1'b0: Disable
0	RG_VMIPI_MODE_SET	**VMIPI low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A7C LDO_VMIPI_CON1 LDO VMIPI Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VMIPI_OCFB_EN	RG_VMIPI_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VMIPI_OCFB_EN	**VMIPI OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VMIPI_OCFB_EN	**Enables VMIPI OCFB** 1'b1: Enable 1'b0: Disable

0A80 LDO_VGP3_CON0 LDO VGP3 Control Register 0 1A60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	DA_QI_VGP3_EN	DA_QI_VGP3_STB						DA_QI_VGP3_MODE					RG_VGP3_ON_CTRL	RG_VGP3_MODE_CTRL	RG_VGP3_EN	RG_VGP3_MODE_SET
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VGP3_EN	**VGP3 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VGP3_STB	
8	DA_QI_VGP3_MODE	**VGP3 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VGP3_ON_CTRL	**Controls VGP3 enable** 1'b0: SW control by RG_VGP3_EN 1'b1: HW control by SRCLKEN
2	RG_VGP3_MODE_CTRL	**Controls VGP3 low power mode** 1'b0: SW control by VGP3_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VGP3_EN	**Enables VGP3** 1'b1: Enable 1'b0: Disable
0	RG_VGP3_MODE_SET	**VGP3 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A82 **LDO_VGP3_CON1** **LDO VGP3 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VGP3_OCFB_EN	RG_VGP3_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VGP3_OCFB_EN	**VGP3 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VGP3_OCFB_EN	**Enables VGP3 OCFB** 1'b1: Enable 1'b0: Disable

0A86 **LDO_VBIF28_CON0** **LDO VBIF28 Control Register 0** **1A60**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VBIF28_EN**	**DA_QI_VBIF28_STB**						**DA_QI_VBIF28_MODE**					**RG_VBIF28_ON_CTRL**	**RG_VBIF28_MODE_CTRL**	**RG_VBIF28_EN**	**RG_VBIF28_MODE_SET**
Type	RO	RO						RO					RW	RW	RW	RW
Reset	0	0						0					0	0	0	0

Bit(s)	Name	Description
15	DA_QI_VBIF28_EN	**VBIF28 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VBIF28_STB	
8	DA_QI_VBIF28_MODE	**VBIF28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VBIF28_ON_CTRL	**Controls VBIF28 enable** 1'b0: SW control by RG_VBIF28_EN 1'b1: HW control by SRCLKEN
2	RG_VBIF28_MODE_CTRL	**Controls VBIF28 low power mode** 1'b0: SW control by VBIF28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VBIF28_EN	**Enables VBIF28** 1'b1: Enable 1'b0: Disable
0	RG_VBIF28_MODE_SET	**VBIF28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A88 **LDO_VBIF28_CON1** **LDO VBIF28 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VBIF28_OCFB_EN**	**RG_VBIF28_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VBIF28_OCFB_EN	**VBIF28 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VBIF28_OCFB_EN	**Enables VBIF28 OCFB** 1'b1: Enable 1'b0: Disable

0A8C **LDO_VEFUSE** **LDO VEFUSE Control Register 0** **0260**

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_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VEFUSE_EN	DA_QI_VEFUSE_STB						DA_QI_VEFUSE_MODE						RG_VEFUSE_MODE_CTRL	RG_VEFUSE_EN	RG_VEFUSE_MODE_SET
Type	RO	RO						RO						RW	RW	RW
Reset	0	0						0						0	0	0

Bit(s)	Name	Description
15	DA_QI_VEFUSE_EN	**VEFUSE enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VEFUSE_STB	
8	DA_QI_VEFUSE_MODE	**VEFUSE low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VEFUSE_MODE_CTRL	**Controls VEFUSE low power mode** 1'b0: SW control by VEFUSE_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VEFUSE_EN	**Enables VEFUSE** 1'b1: Enable 1'b0: Disable
0	RG_VEFUSE_MODE_SET	**VEFUSE low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A8E **LDO_VEFUSE_CON1** **LDO VEFUSE Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VEFUSE_OCFB_EN	RG_VEFUSE_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VEFUSE_OCFB_EN	**VEFUSE OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VEFUSE_OCFB_EN	**Enables VEFUSE OCFB** 1'b1: Enable 1'b0: Disable

0A92 **LDO_VCN33_CON0** **LDO VCN33 Control Register 0** **8260**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	DA_QI_VCN33_EN	DA_QI_VCN33_STB						DA_QI_VCN33_MODE						RG_VCN33_MODE_CTRL		RG_VCN33_MODE_SET
Type	RO	RO						RO						RW		RW
Reset	1	0						0						0		0

Bit(s)	Name	Description
15	DA_QI_VCN33_EN	**VCN33 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VCN33_STB	
8	DA_QI_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCN33_MODE_CTRL	**Controls VCN33 low power mode** 1'b0: SW control by VCN33_MODE_SET 1'b1: HW control by SRCLKEN
0	RG_VCN33_MODE_SET	**VCN33 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A94 LDO_VCN33_CON1 LDO VCN33 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN33_OCFB_EN	RG_VCN33_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN33_OCFB_EN	**VCN33 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VCN33_OCFB_EN	**Enables VCN33 OCFB** 1'b1: Enable 1'b0: Disable

0A9C LDO_VLDO28_CON0 LDO VLDO28 Control Register 0 8260

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VLDO28_EN	DA_QI_VLDO28_STB						DA_QI_VLDO28_MODE					RG_VLDO28_ON_CTRL	RG_VLDO28_MODE_CTRL		RG_VLDO28_MODE_SET
Type	RO	RO						RO					RW	RW		RW
Reset	1	0						0					0	0		0

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Bit(s)	Name	Description
15	DA_QI_VLDO28_EN	**VLDO28 enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VLDO28_STB	
8	DA_QI_VLDO28_MODE	**VLDO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VLDO28_ON_CTRL	**Controls VLDO28 enable** 1'b0: SW control by RG_VLDO28_EN 1'b1: HW control by SRCLKEN
2	RG_VLDO28_MODE_CTRL	**Controls VLDO28 low power mode** 1'b0: SW control by VLDO28_MODE_SET 1'b1: HW control by SRCLKEN
0	RG_VLDO28_MODE_SET	**VLDO28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A9E LDO_VLDO28_CON1 LDO VLDO28 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VLDO28_OCFB_EN**	**RG_VLDO28_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VLDO28_OCFB_EN	**VLDO28 OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VLDO28_OCFB_EN	**Enables VLDO28 OCFB** 1'b1: Enable 1'b0: Disable

0AAA LDO_VMC_CON0 LDO VMC Control Register 0 9A62

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VMC_EN**	**DA_QI_VMC_STB**						**DA_QI_VMC_MODE**					**RG_VMC_ON_CTRL**	**RG_VMC_MODE_CTRL**	**RG_VMC_EN**	**RG_VMC_MODE_SET**
Type	RO	RO						RO					RW	RW	RW	RW
Reset	1	0						0					0	0	1	0

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Bit(s)	Name	Description
15	DA_QI_VMC_EN	**VMC enable status** 1'b1: Enable 1'b0: Disable
14	DA_QI_VMC_STB	
8	DA_QI_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VMC_ON_CTRL	**Controls VMC enable** 1'b0: SW control by RG_VMC_EN 1'b1: HW control by SRCLKEN
2	RG_VMC_MODE_CTRL	**Controls VMC low power mode** 1'b0: SW control by VMC_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VMC_EN	**Enables VMC** 1'b1: Enable 1'b0: Disable
0	RG_VMC_MODE_SET	**VMC low power mode** 1'b0: Normal mode 1'b1: Low power mode

0AAC **LDO_VMC_CON1** **LDO VMC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VMC_OCFB_EN	RG_VMC_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VMC_OCFB_EN	**VMC OCFB status** 1'b1: Over-current occurs. 1'b0: No over-current occurs.
9	RG_VMC_OCFB_EN	**Enables VMC OCFB** 1'b1: Enable 1'b0: Disable

0AB0 **LDO_VMC_CON3** **LDO VMC Control Register 3** **001B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_VMC_TRANS_EN
Type																RW
Reset																1

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Bit(s)	Name	Description
0	RG_VMC_TRANS_EN	**Controls pulse generation** 1'b0: Disable 1'b1: Enable

0ABA VRTC_CON0 VRTC Control Register 0 8002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VRTC_EN**														**RG_VRTC_EN**	
Type	RO														RW	
Reset	1														1	

Bit(s)	Name	Description
15	DA_QI_VRTC_EN	**VRTC enable status**
1	RG_VRTC_EN	**Enables VRTC** 1'b1: Enable 1'b0: Disable

0AC4 VXO22_ANA_CON0 VXO22 Control Register 0 0A00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VXO22_NDIS_EN**		**RG_VXO22_VOSEL**						**RG_VXO22_CAL**			
Type					RW		RW						RW			
Reset					1		1	0					0	0	0	0

Bit(s)	Name	Description
11	RG_VXO22_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
9:8	RG_VXO22_VOSEL	**Selects LDO voltage** 2'b10: 2.2V
3:0	RG_VXO22_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV

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Bit(s)	Name	Description
		4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AC6 **VTCXO28_ANA_CON0** **VTCXO28 Control Register 0** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_VTCXO28_VOSEL						RG_VTCXO28_CAL			
Type							RW						RW			
Reset							0	0					0	0	0	0

Bit(s)	Name	Description
9:8	RG_VTCXO28_VOSEL	**Selects LDO voltage** 2'b00: 2.8V
3:0	RG_VTCXO28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AC8 **VTCXO24_ANA_CON0** **VTCXO24 Control Register 0** **0900**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VTCXO24_NDIS_EN		RG_VTCXO24_VOSEL						RG_VTCXO24_CAL			
Type					RW		RW						RW			
Reset					1		0	1					0	0	0	0

Bit(s)	Name	Description
11	RG_VTCXO24_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
9:8	RG_VTCXO24_VOSEL	**Selects LDO voltage** 2'b01: 2.375V

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Bit(s)	Name	Description
3:0	RG_VTCXO24_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0ACA **VBIF28_ANA_CON0** **VBIF28 Control Register 0** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VBIF28_CAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VBIF28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0ACC **VCN28_ANA_CON0** **VCN28 Control Register 0** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN28_NDI		RG_VCN28_VOSEL						RG_VCN28_CAL			

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					S_EN											
Type					RW		RW						RW			
Reset					1		0	0					0	0	0	0

Bit(s)	Name	Description
11	RG_VCN28_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
9:8	RG_VCN28_VOSEL	**Selects LDO voltage** 2'b00: 2.8V
3:0	RG_VCN28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0ACE **VMCH_ANA_CON0** **VMCH Control Register 0** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VMCH_VOSEL				RG_VMCH_CAL				
Type								RW				RW				
Reset								0				0	0	1	0	1

Bit(s)	Name	Description
8	RG_VMCH_VOSEL	**Output selection signal** (1'b0: 3.0V) 1'b0: 2.9V (and 0xACE[4:0]=5'h5) 1'b0: 3.0V (and 0xACE[4:0]=5'h0) 1'b1: 3.3V (and 0xACE[4:0]=5'h0)
4:0	RG_VMCH_CAL	**Calibrates LDO voltage** (5'b00000: 0mV) 5'b00000: 0mV 5'b00001: -20mV 5'b00010: -40mV 5'b00011: -60mV 5'b00100: -80mV 5'b00101: -100mV 5'b00110: -120mV

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Bit(s)	Name	Description
		5'b00111: -140mV 5'b01000: -160mV 5'b01001: -180mV 5'b01010: -200mV 5'b01011: -220mV 5'b01100: -240mV 5'b01101: -260mV 5'b01110: -280mV 5'b01111: -300mV 5'b00000: 0mV 5'b10001: +320mV 5'b10010: +280mV 5'b10011: +260mV 5'b10100: +240mV 5'b10101: +220mV 5'b10110: +200mV 5'b10111: +180mV 5'b11000: +160mV 5'b11001: +150mV 5'b11010: +120mV 5'b11011: +100mV 5'b11100: +80mV 5'b11101: +60mV 5'b11110: +40mV 5'b11111: +20mV

0AD0 **VMCH_ANA_CON1** **VMCH Control Register 1** **0022**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VMCH_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VMCH_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AD2 **VEMC_ANA_CON0** **VEMC Control Register 0** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VEMC_VOSEL				RG_VEMC_CAL				
Type								RW				RW				
Reset								0				0	0	1	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
8	RG_VEMC_VOSEL	**Output selection signal** (1'b0: 3V) 1'b0: 2.9V (and 0xAD2[4:0]=5'h5) 1'b0: 3.0V (and 0xAD2[4:0]=5'h0) 1'b1: 3.3V (and 0xAD2[4:0]=5'h0)
4:0	RG_VEMC_CAL	**Calibrates LDO voltage** (5'b00000: 0mV) 5'b00000: 0mV 5'b00001: -20mV 5'b00010: -40mV 5'b00011: -60mV 5'b00100: -80mV 5'b00101: -100mV 5'b00110: -120mV 5'b00111: -140mV 5'b01000: -160mV 5'b01001: -180mV 5'b01010: -200mV 5'b01011: -220mV 5'b01100: -240mV 5'b01101: -260mV 5'b01110: -280mV 5'b01111: -300mV 5'b00000: 0mV 5'b10001: +320mV 5'b10010: +280mV 5'b10011: +260mV 5'b10100: +240mV 5'b10101: +220mV 5'b10110: +200mV 5'b10111: +180mV 5'b11000: +160mV 5'b11001: +150mV 5'b11010: +120mV 5'b11011: +100mV 5'b11100: +80mV 5'b11101: +60mV 5'b11110: +40mV 5'b11111: +20mV

0AD4 **VEMC_ANA_CON1** **VEMC Control Register 1** **0022**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VEMC_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VEMC_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

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0AD6 **VCAMA_ANA_CON0** **VCAMA Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCAMA_VOSEL							RG_VCAMA_CAL			
Type						RW							RW			
Reset						0	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VCAMA_VOSEL	**Selects output voltage** (3'b011: 2.8V) 3'b011: 2.8V
3:0	RG_VCAMA_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AD8 **VCAMA_ANA_CON1** **VCAMA Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VCAMA_FBSEL		RG_VCAMA_NDIS_EN	
Type													RW		RW	
Reset													0	0	1	

Bit(s)	Name	Description
3:2	RG_VCAMA_FBSEL	**Selects load regulation performance** 2'b00: 18mV 2'b01: 8mV 2b'10: 12mV 2b'11: 30mV
1	RG_VCAMA_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

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0ADA	VCN33_ANA_CON0	VCN33 Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCN33_VOSEL						RG_VCN33_CAL				
Type						RW						RW				
Reset						0	0					0	0	0	0	0

Bit(s)	Name	Description
10:9	RG_VCN33_VOSEL	**Selects output voltage** (2'b00: 3.3V) 2'b00: 3.3V 2'b01: 3.4V 2'b10: 3.5V 2'b11: 3.6V
4:0	RG_VCN33_CAL	**Calibrates LDO voltage** (5'b00000: 0mV) 5'b00000: 0mV 5'b00001: -20mV 5'b00010: -40mV 5'b00011: -60mV 5'b00100: -80mV 5'b00101: -100mV 5'b00110: -120mV 5'b00111: -140mV 5'b01000: -160mV 5'b01001: -180mV 5'b01010: -200mV 5'b01011: -220mV 5'b01100: -240mV 5'b01101: -260mV 5'b01110: -280mV 5'b01111: -300mV 5'b00000: 0mV 5'b10001: +320mV 5'b10010: +280mV 5'b10011: +260mV 5'b10100: +240mV 5'b10101: +220mV 5'b10110: +200mV 5'b10111: +180mV 5'b11000: +160mV 5'b11001: +150mV 5'b11010: +120mV 5'b11011: +100mV 5'b11100: +80mV 5'b11101: +60mV 5'b11110: +40mV 5'b11111: +20mV

0ADC	VCN33_ANA_CON1	VCN33 Control Register 1	0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VCN33	

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															_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VCN33_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0ADE **VIO28_ANA_CON0** **VIO28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VIO28_VOSEL							RG_VIO28_CAL			
Type						RW							RW			
Reset						0	0	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VIO28_VOSEL	**Output selection signal** (3'b000: 2.8V) 3'b000: 2.8V 3'b001: 2.8V 3'b010: 2.8V 3'b011: 2.8V 3'b100: 2.8V 3'b101: 2.8V 3'b110: 2.8V 3'b111: 2.8V
3:0	RG_VIO28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40V 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AE0 **VIO28_ANA_CON1** **VIO28 Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VIO28	

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															_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VIO28_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AE2 **VMC_ANA_CON0** **VMC Control Register 0** **051B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VMC_VOSEL						RG_VMC_CAL				
Type						RW						RW				
Reset						1	0	1				1	1	0	1	1

Bit(s)	Name	Description
10:8	RG_VMC_VOSEL	**Output selection signal** (3'b101: 2.8V) 3'b011: 1.8V 3'b101: 2.9V (and 0xAE2[4:0]=5'h1B) 3'b110: 3.0V 3'b111: 3.3V
4:0	RG_VMC_CAL	**Calibrates LDO voltage** (5'b00000: 0mV) 5'b00000: 0mV 5'b00001: -20mV 5'b00010: -40mV 5'b00011: -60mV 5'b00100: -80mV 5'b00101: -100mV 5'b00110: -120mV 5'b00111: -140mV 5'b01000: -160mV 5'b01001: -180mV 5'b01010: -200mV 5'b01011: -220V 5'b01100: -240mV 5'b01101: -260mV 5'b01110: -280mV 5'b01111: -300mV 5'b00000: 0mV 5'b10001: +300mV 5'b10010: +280mV 5'b10011: +260mV 5'b10100: +240mV 5'b10101: +220mV 5'b10110: +200mV 5'b10111: +180mV 5'b11000: +160mV 5'b11001: +140mV 5'b11010: +120mV 5'b11011: +100mV 5'b11100: +80mV 5'b11101: +60mV

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Bit(s)	Name	Description
		5'b11110: +40mV 5'b11111: +20mV

0AE4 VMC_ANA_CON1 VMC Control Register 1 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VMC_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VMC_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AE6 VIBR_ANA_CON0 VIBR Control Register 0 0500

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VIBR_VOSEL							RG_VIBR_CAL			
Type						RW							RW			
Reset						1	0	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VIBR_VOSEL	**Output selection signal** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V
3:0	RG_VIBR_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV

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Bit(s)	Name	Description
		4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AE8 **VIBR_ANA_CON1** **VIBR Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VIBR_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VIBR_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AEA **VUSB33_ANA_CON0** **VUSB33 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VUSB33_CAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VUSB33_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AEC **VUSB33_ANA_CON1** **VUSB33 Control Register 1** **0022**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VUSB33_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VUSB33_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AEE **VSIM1_ANA_CON0** **VSIM1 Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VSIM1_VOSEL							RG_VSIM1_CAL			
Type						RW							RW			
Reset						0	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VSIM1_VOSEL	**Output selection signal** 3'b000 &RG_EFUSE_SIM1_MODE=0: 1.2V (not verified) 3'b001 &RG_EFUSE_SIM1_MODE=0: 1.3V(not verified) 3'b010 &RG_EFUSE_SIM1_MODE=0: 1.7V 3'b011 &RG_EFUSE_SIM1_MODE=0: 1.8V 3'b100 &RG_EFUSE_SIM1_MODE=0: 1.86V 3'b101 &RG_EFUSE_SIM1_MODE=0: 2.76V 3'b110 &RG_EFUSE_SIM1_MODE=0: 3.0V 3'b111 &RG_EFUSE_SIM1_MODE=0: 3.1V 3'b000 &RG_EFUSE_SIM1_MODE=1: 1.2V (not verified) 3'b001 &RG_EFUSE_SIM1_MODE=1: 1.3V (not verified) 3'b010 &RG_EFUSE_SIM1_MODE=1: 1.7V 3'b011 &RG_EFUSE_SIM1_MODE=1: 1.8V 3'b100 &RG_EFUSE_SIM1_MODE=1: 1.9V (not verified) 3'b101 &RG_EFUSE_SIM1_MODE=1: 2.0V (not verified) 3'b110 &RG_EFUSE_SIM1_MODE=1: 2.1V (not verified) 3'b111 &RG_EFUSE_SIM1_MODE=1: 2.2V (not verified)
3:0	RG_VSIM1_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV

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Bit(s)	Name	Description
		4'b1110: +40mV 4'b1111: +20mV

0AF0 **VSIM1_ANA_CON1** **VSIM1 Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VSIM1_STB_CAL						RG_VSIM1_NDIS_EN	
Type									RW						RW	
Reset									0	0					1	

Bit(s)	Name	Description
7:6	RG_VSIM1_STB_CAL	**Not in use**
1	RG_VSIM1_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AF2 **VSIM2_ANA_CON0** **VSIM2 Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VSIM2_VOSEL							RG_VSIM2_CAL			
Type						RW							RW			
Reset						0	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VSIM2_VOSEL	**Output selection signal** 3'b010 &RG_EFUSE_VSIM2_MODE=0: 1.7V 3'b011 &RG_EFUSE_VSIM2_MODE=0: 1.8V 3'b100 &RG_EFUSE_VSIM2_MODE=0: 1.86V 3'b101 &RG_EFUSE_VSIM2_MODE=0: 2.76V 3'b110 &RG_EFUSE_VSIM2_MODE=0: 3.0V 3'b111 &RG_EFUSE_VSIM2_MODE=0: 3.1V 3'b010 &RG_EFUSE_VSIM2_MODE=1: 1.7V 3'b011 &RG_EFUSE_VSIM2_MODE=1: 1.8V
3:0	RG_VSIM2_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV

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Bit(s)	Name	Description
		4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AF4 VSIM2_ANA_CON1 VSIM2 Control Register 1 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VSIM2_STB_CAL						RG_VSIM2_NDIS_EN	
Type									RW						RW	
Reset									0	0					1	

Bit(s)	Name	Description
7:6	RG_VSIM2_STB_CAL	**Calibrates soft start current to modify soft start time** 2'b00: Slow 2'b11: Fast
1	RG_VSIM2_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AF6 VEFUSE_ANA_CON0 VEFUSE Control Register 0 0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VEFUSE_VOSEL							RG_VEFUSE_CAL			
Type						RW							RW			
Reset						0	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VEFUSE_VOSEL	**Output selection signal** 3'b010 &RG_EFUSE_MODE_1=0: 1.7V 3'b011 &RG_EFUSE_MODE_1=0: 1.8V 3'b010 &RG_EFUSE_MODE_1=1: 1.71V 3'b011 &RG_EFUSE_MODE_1=1: 1.8V 3'b100 &RG_EFUSE_MODE_1=1: 1.89V 3'b101 &RG_EFUSE_MODE_1=1: 2.0V 3'b110 &RG_EFUSE_MODE_1=1: 2.1V 3'b111 &RG_EFUSE_MODE_1=1: 2.2V
3:0	RG_VEFUSE_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV

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Bit(s)	Name	Description
		4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AF8 **VEFUSE_ANA_CON1** **VEFUSE Control Register 1** **4002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VEFUSE_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VEFUSE_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0AFA **VA18_ANA_CON0** **VA18 Control Register 0** **0B00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VA18_NDIS_EN		RG_VA18_VOSEL						RG_VA18_CAL			
Type					RW		RW						RW			
Reset					1		1	1					0	0	0	0

Bit(s)	Name	Description
11	RG_VA18_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
9:8	RG_VA18_VOSEL	**Selects LDO voltage** 2'b11: 1.8V
3:0	RG_VA18_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV

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Bit(s)	Name	Description
		4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0AFC VGP3_ANA_CON0 VGP3 Control Register 0 0700

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VGP3_VOSEL							RG_VGP3_CAL			
Type						RW							RW			
Reset						1	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VGP3_VOSEL	**Output selection signal** 3'b000: 1.0V 3'b001: 1.05V 3'b010: 1.1V 3'b011: 1.22V 3'b100: 1.3V 3'b101: 1.5V 3'b110: 1.8V 3'b111: 1.81V
3:0	RG_VGP3_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0AFE VGP3_ANA_CON1 VGP3 Control Register 1 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VGP3_NDIS_EN	
Type															RW	

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Reset															1	

Bit(s)	Name	Description
1	RG_VGP3_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B00 VCAMD_ANA_CON0 VCAMD Control Register 0 0500

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_VCAMD_VOSEL**						**RG_VCAMD_CAL**				
Type						RW						RW				
Reset						1	0	1				0	0	0	0	0

Bit(s)	Name	Description
10:8	RG_VCAMD_VOSEL	**Output selection signal** 3'b000: 0.9V 3'b010: 1.0V 3'b011: 1.05V 3'b100: 1.1V 3'b110: 1.21V 3'b111: 1.21V
4:0	RG_VCAMD_CAL	**Calibrates LDO voltage** (5'b0000: 0mV) 5'b00000: 0mV 5'b00001: -10mV 5'b00010: -20mV 5'b00011: -30mV 5'b00100: -40mV 5'b00101: -50mV 5'b00110: -60mV 5'b00111: -70mV 5'b01000: -80mV 5'b01001: -90mV 5'b01010: -100mV 5'b01011: -110mV 5'b01100: -120mV 5'b01101: -130mV 5'b01110: -140mV 5'b01111: -150mV 5'b10000: +160mV 5'b10001: +150mV 5'b10010: +140mV 5'b10011: +130mV 5'b10100: +120mV 5'b10101: +110mV 5'b10110: +100mV 5'b10111: +90mV 5'b11000: +80mV 5'b11001: +70mV 5'b11010: +60mV 5'b11011: +50mV 5'b11100: +40mV 5'b11101: +30mV

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Bit(s)	Name	Description
		5'b11110: +20mV 5'b11111: +10mV

0B02 **VCAMD_ANA_CON1** **VCAMD Control Register 1** **003E**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VCAMD_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VCAMD_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B04 **VIO18_ANA_CON0** **VIO18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VIO18_CAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VIO18_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B06 **VIO18_ANA_CON1** **VIO18 Control Register 1** **0012**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_VIO18_NDIS_EN**	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VIO18_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B08 VRF18_ANA_CON0 VRF18 Control Register 0 0700

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_VRF18_VOSEL**							**RG_VRF18_CAL**			
Type						RW							RW			
Reset						1	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VRF18_VOSEL	**Output selection signal** 3'b111: 1.81V
3:0	RG_VRF18_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B0A VRF18_ANA_CON1 VRF18 Control Register 1 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_VRF18_NDIS_EN**	
Type															RW	
Reset															1	

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Bit(s)	Name	Description
1	RG_VRF18_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B0C **VRF12_ANA_CON0** **VRF12 Control Register 0** **0400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VRF12_VOSEL							RG_VRF12_CAL			
Type						RW							RW			
Reset						1	0	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VRF12_VOSEL	**Output selection signal** (3'b111: 1.8V) 3'b100: 1.2V
3:0	RG_VRF12_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B0E **VRF12_ANA_CON1** **VRF12 Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VRF12_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VRF12_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

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0B10 **VA10_ANA_CON0** **VA10 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VA10_VOSEL							RG_VA10_CAL			
Type						RW							RW			
Reset						0	0	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VA10_VOSEL	**Output selection signal** (3'b111: 1.8V) 3'b000: 0.9V 3'b001: 0.95V 3'b010: 1V
3:0	RG_VA10_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B12 **VA10_ANA_CON1** **VA10 Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VA10_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VA10_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B14 **VCAMIO_ANA_CON0** **VCAMIO Control Register 0** **0600**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name						RG_VCAMIO_VOSEL							RG_VCAMIO_CAL			
Type						RW							RW			
Reset						1	1	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VCAMIO_VOSEL	**Output selection signal** (3'b111: 1.8V) 3'b000: 0.9V 3'b001: 0.95V 3'b010: 1V 3'b011: 1.05V 3'b100: 1.2V 3'b101: 1.5V 3'b110: 1.8V 3'b111: No use
3:0	RG_VCAMIO_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B16 **VCAMIO_ANA_CON1** **VCAMIO Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VCAMIO_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VCAMIO_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B18 **VCN18_ANA_CON0** **VCN18 Control Register 0** **0600**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCN18_VOSEL							RG_VCN18_CAL			
Type						RW							RW			
Reset						1	1	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VCN18_VOSEL	**Output selection signal** (3'b111: 1.8 V) 3'b000: 0.9V 3'b001: 0.95V 3'b010: 1V 3'b011: 1.05V 3'b100: 1.2V 3'b101: 1.5V 3'b110: 1.8V 3'b111: No use
3:0	RG_VCN18_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B1A **VCN18_ANA_CON1** **VCN18 Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VCN18_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VCN18_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B1C **VMIPI_ANA_CON0** **VMIPI Control Register 0** **0600**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VMIPI_VOSEL							RG_VMIPI_CAL			
Type						RW							RW			
Reset						1	1	0					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VMIPI_VOSEL	**Output selection signal** (3'b111: 1.8V) 3'b000: 0.9V 3'b001: 0.95V 3'b010: 1V 3'b011: 1.05V 3'b100: 1.2V 3'b101: 1.5V 3'b110: 1.8V 3'b111: No use
3:0	RG_VMIPI_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -10mV 4'b0010: -20mV 4'b0011: -30mV 4'b0100: -40mV 4'b0101: -50mV 4'b0110: -60mV 4'b0111: -70mV 4'b1000: +80mV 4'b1001: +70mV 4'b1010: +60mV 4'b1011: +50mV 4'b1100: +40mV 4'b1101: +30mV 4'b1110: +20mV 4'b1111: +10mV

0B1E **VMIPI_ANA_CON1** **VMIPI Control Register 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VMIPI_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VMIPI_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B20 **VSRAM_PROC_ANA_CON1** **VSRAM_PROC Control Register 1** **0022**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VSRAM_PROC_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VSRAM_PROC_NDIS_EN	**Enables LDO output power down NMOS discharge** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B22 **VDRAM_ANA_CON0** **VDRAM Control Register 0** **0600**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VDRAM_VOSEL						RG_VDRAM_CAL				
Type						RW						RW				
Reset						1	1	0				0	0	0	0	0

Bit(s)	Name	Description
10:8	RG_VDRAM_VOSEL	**Output selection signal** 3'b000: 0.9V 3'b001: 0.95V 3'b010: 1.0V 3'b011: 1.05V 3'b100: 1.1V 3'b101: 1.2V 3'b110: 1.21V 3'b111: 1.21V
4:0	RG_VDRAM_CAL	**D => A calibrates LDO voltage** (5'b0000: 0mV) 5'b00000: 0mV 5'b00001: -10mV 5'b00010: -20mV 5'b00011: -30mV 5'b00100: -40mV 5'b00101: -50mV 5'b00110: -60mV 5'b00111: -70mV 5'b01000: -80mV 5'b01001: -90mV 5'b01010: -100mV 5'b01011: -110mV 5'b01100: -120mV 5'b01101: -130mV 5'b01110: -140mV 5'b01111: -150mV 5'b10000: +160mV 5'b10001: +150mV 5'b10010: +140mV 5'b10011: +130mV 5'b10100: +120mV 5'b10101: +110mV

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Bit(s)	Name	Description
		5'b10110: +100mV 5'b10111: +90mV 5'b11000: +80mV 5'b11001: +70mV 5'b11010: +60mV 5'b11011: +50mV 5'b11100: +40mV 5'b11101: +30mV 5'b11110: +20mV 5'b11111: +10mV

0B24 **VDRAM_ANA_CON1** **VDRAM Control Register 1** **003E**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VDRAM_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VDRAM_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B26 **VLDO28_ANA_CON0** **VLDO28 Control Register 0** **000A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_VLDO28_CAL				
Type												RW				
Reset												0	1	0	1	0

Bit(s)	Name	Description
4:0	RG_VLDO28_CAL	**Calibrates LDO voltage** (5'b00000: 0mV) 5'b00000: 0mV 5'b00001: -20V 5'b00010: -40mV 5'b00011: -60mV 5'b00100: -80mV 5'b00101: -100mV 5'b00110: -120mV 5'b00111: -140mV 5'b01000: -160mV 5'b01001: -180mV 5'b01010: -200mV 5'b01011: -220mV 5'b01100: 240mV 5'b01101: -260mV 5'b01110: -280mV

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Bit(s)	Name	Description
		5'b01111: -300mV 5'b00000: 0mV 5'b10001: +320mV 5'b10010: +280mV 5'b10011: +260mV 5'b10100: +240mV 5'b10101: +220mV 5'b10110: +200mV 5'b10111: +180mV 5'b11000: +160mV 5'b11001: +150mV 5'b11010: +120mV 5'b11011: +100mV 5'b11100: +80mV 5'b11101: +60mV 5'b11110: +40mV 5'b11111: +20mV

0B28 **VLDO28_ANA_CON1** **VLDO28 Control Register 1** **0022**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VLDO28_NDIS_EN	
Type															RW	
Reset															1	

Bit(s)	Name	Description
1	RG_VLDO28_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down

0B2A **BIF_CON0** **BIF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_0										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_0	Command queue 0

0B2C **BIF_CON1** **BIF Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_1										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
10:0	BIF_COMMAND_1	Command queue 1

0B2E **BIF_CON2** **BIF Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_2										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_2	Command queue 2

0B30 **BIF_CON3** **BIF Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_3										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_3	Command queue 3

0B32 **BIF_CON4** **BIF Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_4										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_4	Command queue 4

0B34 **BIF_CON5** **BIF Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_5										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_5	Command queue 5

0B36 **BIF_CON6** **BIF Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name						**BIF_COMMAND_6**										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_6	Command queue 6

0B38 BIF_CON7 BIF Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**BIF_COMMAND_7**										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_7	Command queue 7

0B3A BIF_CON8 BIF Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**BIF_COMMAND_8**										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_8	Command queue 8

0B3C BIF_CON9 BIF Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**BIF_COMMAND_9**										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_9	Command queue 9

0B3E BIF_CON10 BIF Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**BIF_COMMAND_10**										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_10	Command queue 10

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0B40 BIF_CON11 BIF Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_11										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_11	Command queue 11

0B42 BIF_CON12 BIF Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_12	Command queue 12

0B44 BIF_CON13 BIF Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_13										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_13	Command queue 13

0B46 BIF_CON14 BIF Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_14										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_14	Command queue 14

0B48 BIF_CON15 BIF Control Register 15 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TRASFER_NUM						BIF_COMMAND_TYPE									
Type	RW						RW									
Reset	0	1	0	0			0	0								

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Bit(s)	Name	Description
15:12	BIF_TRASFER_NUM	**Total transfer number in command queue**
9:8	BIF_COMMAND_TYPE	**Command type** 2'b00: Write 2'b01: Read data 2'b10: Read response

0B4A BIF_CON16 BIF Control Register 16 1431

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_STOP_SET							BIF_LOGIC_1_SET					BIF_LOGIC_0_SET			
Type	RW							RW					RW			
Reset	0	0	0	1	0	1		0	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
15:10	BIF_STOP_SET	**Sets up stop signal spec** 6'd0: 0T 6'd1: 1T 6'd2: 2T 6'dN: NT
8:4	BIF_LOGIC_1_SET	**Sets up logic "1" period spec** 5'd0: 0T 5'd1: 1T 5'd2: 2T 5'dN: NT
3:0	BIF_LOGIC_0_SET	**Sets up logic "0" period spec** 4'd0: 0T 4'd1: 1T 4'd2: 2T 4'dN: NT

0B4C BIF_CON17 BIF Control Register 17 1011

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_READ_EXPECT_NUM											BIF_DEBOUNCE_EN	BIF_DEBOUNCE_THD		BIF_DEBOUNCE_WND	
Type	RW											RW	RW		RW	
Reset	0	0	0	1								1	0	0	0	1

Bit(s)	Name	Description
15:12	BIF_READ_EXPECT_NUM	**Expects the number of Read back data** 0: 0 1: 1 data packege
4	BIF_DEBOUNCE_EN	**Enables debounce function** 1'b0: Disable 1'b1: Enable
3:2	BIF_DEBOUNCE_THD	**Threshold setting in decision windows** 2'b00: 4/8 2'b01: 3/8

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Bit(s)	Name	Description
		2'b10: 2/8 2'b11: 1/8
1:0	BIF_DEBOUNCE_WND	**Decision window setting** 2'b00: 16us 2'b01: 32us 2'b10: 64us 2'b11: 128us

0B4E **BIF_CON18** **BIF Control Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BIF_TRASACT_TRIGGER**
Type																RW
Reset																0

Bit(s)	Name	Description
0	BIF_TRASACT_TRIGGER	**Trigger signal** 1'b1: Trigger BIF module

0B50 **BIF_CON19** **BIF Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**BIF_RESPONSE**									**BIF_DATA_NUM**			
Type				RO									RO			
Reset				0									0	0	0	0

Bit(s)	Name	Description
12	BIF_RESPONSE	**Response result** 1'b1: Positive response 1'b0: Negative response
3:0	BIF_DATA_NUM	**Number of Read back data**

0B52 **BIF_CON20** **BIF Control Register 20** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BIF_ERROR_0**							**BIF_ACK_0**	**BIF_DATA_0**							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_0	**Error happens or not** 1'b1: Error exists.

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Bit(s)	Name	Description
		1'b0: No error
8	BIF_ACK_0	
7:0	BIF_DATA_0	**Read back data**

0B54 BIF_CON21 BIF Control Register 21 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_1							BIF_ACK_1	BIF_DATA_1							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_1	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_1	
7:0	BIF_DATA_1	**Read back data**

0B56 BIF_CON22 BIF Control Register 22 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_2							BIF_ACK_2	BIF_DATA_2							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_2	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_2	
7:0	BIF_DATA_2	**Read back data**

0B58 BIF_CON23 BIF Control Register 23 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_3							BIF_ACK_3	BIF_DATA_3							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_3	**Error happens or not** 1'b1: Error exists.

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Bit(s)	Name	Description
		1'b0: No error
8	BIF_ACK_3	
7:0	BIF_DATA_3	**Read back data**

0B5A BIF_CON24 BIF Control Register 24 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_4							BIF_ACK_4	BIF_DATA_4							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_4	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_4	
7:0	BIF_DATA_4	**Read back data**

0B5C BIF_CON25 BIF Control Register 25 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_5							BIF_ACK_5	BIF_DATA_5							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_5	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_5	
7:0	BIF_DATA_5	**Read back data**

0B5E BIF_CON26 BIF Control Register 26 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_6							BIF_ACK_6	BIF_DATA_6							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_6	**Error happens or not** 1'b1: Error exists.

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Bit(s)	Name	Description
		1'b0: No error
8	BIF_ACK_6	
7:0	BIF_DATA_6	**Read back data**

0B60 BIF_CON27 BIF Control Register 27 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_7							BIF_ACK_7	BIF_DATA_7							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_7	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_7	
7:0	BIF_DATA_7	**Read back data**

0B62 BIF_CON28 BIF Control Register 28 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_8							BIF_ACK_8	BIF_DATA_8							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_8	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_8	
7:0	BIF_DATA_8	**Read back data**

0B64 BIF_CON29 BIF Control Register 29 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_9							BIF_ACK_9	BIF_DATA_9							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_9	**Error happens or not** 1'b1: Error exists.

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Bit(s)	Name	Description
		1'b0: No error
8	BIF_ACK_9	
7:0	BIF_DATA_9	**Read back data**

0B68 **BIF_CON31** **BIF Control Register 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BIF_BUS_STATUS**	**BIF_TOTAL_VALID**	**BIF_BAT_LOST**	**BIF_TIMEOUT**	**BIF_IRQ**	**BIF_BAT_LOST_GATED**									**BIF_IRQ_CLR**	**BIF_BACK_NORMAL**
Type	RO	RO	RO	RO	RO	RO									RW	RW
Reset	0	0	0	0	0	0									0	0

Bit(s)	Name	Description
15	BIF_BUS_STATUS	**busy: BIF is still in action** 1'b0: Complete 1'b1: Busy
14	BIF_TOTAL_VALID	**Error happens or not in all read data** 1'b1: Error exists (for all data). 1'b0: No error
13	BIF_BAT_LOST	1'b0: Battery exists. 1'b1: Battery undetected
12	BIF_TIMEOUT	1'b1: Timeout
11	BIF_IRQ	**BIF interrupt status** Because this register is cleared by HW, the interrupt edge-sensitive scheme should be adopted for this design. 1'b1: Interrupt issued
10	BIF_BAT_LOST_GATED	1'b0: Battery exists. 1'b1: Battery undetected
1	BIF_IRQ_CLR	**Clears BIF interrupt status** When BIF interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status.
0	BIF_BACK_NORMAL	**Finishes interrupt mode** 1'b1: Abort interrupt mode

0B6A **BIF_CON32** **BIF Control Register 32** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BIF_POWER_UP**											**BIF_POWER_UP_COUNT**				
Type	RW											RW				
Reset	0											1	0	0	0	0

Bit(s)	Name	Description
15	BIF_POWER_UP	1'b1: Power up slave device
4:0	BIF_POWER_UP_CO	**Powers up counter setting**

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Bit(s)	Name	Description
	UNT	5'd0: 0 5'd1: 1T 5'd2: 2T 5'dN: NT

0B74 BIF_BAT_CON0 BIF_BATON Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BATON_HT_EN_DLY_TIME				RG_BATON_HT_EN
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	RG_BATON_HT_EN_DLY_TIME	**BATON high-temperature detection delay time** 1'b0: 6T 1'b1: 12T
0	RG_BATON_HT_EN	**Detects Battery-On HW high temperature** 1'b0: Disable 1'b1: Enable

0B76 BIF_CON37 BIF Control Register 37 000B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TIMEOUT_SET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
15:0	BIF_TIMEOUT_SET	**Sets up timeout spec** 16'd0: 0T 16'd1: 1T 16'd2: 2T 16'dN: NT

0B78 BIF_CON38 BIF Control Register 38 8022

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_RX_DEG_EN						BIF_RX_DEG_WND									
Type	RW						RW									
Reset	1						0	0	0	0	1	0	0	0	1	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	BIF_RX_DEG_EN	**Enables deglitch** 1'b0: Bypass 1'b1: Enable HW deglitch
9:0	BIF_RX_DEG_WND	**Filter window** 10'd0: 1T 10'd1: 2T 10'd2: 3T 10'dN: (N+1)T

0C00 OTP_CON0 OTP Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_OTP_PA					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	RG_OTP_PA	OTP PA

0C02 OTP_CON1 OTP Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_OTP_PDIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_OTP_PDIN	OTP PDIN

0C04 OTP_CON2 OTP Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PTM	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PTM	OTP PTM

0C06 OTP_CON3 OTP Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PWE	
Type															RW	
Reset															0	0

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Bit(s)	Name	Description
1:0	RG_OTP_PWE	OTP PWE

0C08 OTP_CON4 OTP Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_PPROG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PPROG	OTP PPROG

0C0A OTP_CON5 OTP Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_PWE_SRC
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PWE_SRC	**Selects OTP write (fusing) PWE source** 0: From IO pad 1: From register

0C0C OTP_CON6 OTP Control Register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_PROG_PKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_PROG_PKEY	OTP write (fusing) match key

0C0E OTP_CON7 OTP Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_RD_PKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_RD_PKEY	OTP read match key

0C10 OTP_CON8 OTP Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_TRIG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_TRIG	OTP SW read trigger

0C12 OTP_CON9 OTP Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_RD_RDY_BYPASS
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_RD_RDY_BYPASS	**Bypasses OTP read ready delay** 0: Does not bypass 1: Bypass

0C14 OTP_CON10 OTP Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_SKIP_OTP_OUT
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_SKIP_OTP_OUT	**Skips reading from EFUSE macro** 0: Does not skip 1: Skip

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0C16 OTP_CON11 OTP Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_SW
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_SW	**SW trigger read mode** 0: Not SW trigger read mode 1: SW trigger read mode

0C18 OTP_CON12 OTP Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_SW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_SW	Cuurent SW trigger read value

0C1A OTP_CON13 OTP Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_OTP_RD_ACK		RG_OTP_RD_BUSY
Type														RO		RO
Reset														0		0

Bit(s)	Name	Description
2	RG_OTP_RD_ACK	OTP read ack
0	RG_OTP_RD_BUSY	OTP busy status

0C1C OTP_CON14 OTP Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_OTP_PA_SW				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RG_OTP_PA_SW	Current SW trigger read row

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0C1E **OTP_DOUT_0_15** **OTP dout 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_0_15	

0C20 **OTP_DOUT_16_31** **OTP dout 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_16_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_16_31	

0C22 **OTP_DOUT_32_47** **OTP dout 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_32_47															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_32_47	

0C24 **OTP_DOUT_48_63** **OTP dout 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_48_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_48_63	

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0C26 **OTP_DOUT_64_79** **OTP dout 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_64_79															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_64_79	

0C28 **OTP_DOUT_80_95** **OTP dout 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_80_95															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_80_95	

0C2A **OTP_DOUT_96_111** **OTP dout 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_96_111															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_96_111	

0C2C **OTP_DOUT_112_127** **OTP dout 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_112_127															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_112_127	

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0C2E **OTP_DOUT_128_143** **OTP dout 128 143** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_128_143															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_128_143	

0C30 **OTP_DOUT_144_159** **OTP dout 144 159** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_144_159															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_144_159	

0C32 **OTP_DOUT_160_175** **OTP dout 160 175** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_160_175															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_160_175	

0C34 **OTP_DOUT_176_191** **OTP dout 176 191** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_176_191															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_176_191	

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0C36 **OTP_DOUT_192_207** **OTP dout 192 207** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_192_207															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_192_207	

0C38 **OTP_DOUT_208_223** **OTP dout 208 223** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_208_223															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_208_223	

0C3A **OTP_DOUT_224_239** **OTP dout 224 239** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_224_239															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_224_239	

0C3C **OTP_DOUT_240_255** **OTP dout 240 255** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_240_255															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_240_255	

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0C3E **OTP_DOUT_256_271** **OTP dout 256 271** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_256_271															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_256_271	

0C40 **OTP_DOUT_272_287** **OTP dout 272 287** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_272_287															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_272_287	

0C42 **OTP_DOUT_288_303** **OTP dout 288 303** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_288_303															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_288_303	

0C44 **OTP_DOUT_304_319** **OTP dout 304 319** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_304_319															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_304_319	

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0C46 OTP_DOUT_320_335 OTP dout 320 335 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_320_335															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_320_335	

0C48 OTP_DOUT_336_351 OTP dout 336 351 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_336_351															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_336_351	

0C4A OTP_DOUT_352_367 OTP dout 352 367 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_352_367															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_352_367	

0C4C OTP_DOUT_368_383 OTP dout 368 383 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_368_383															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_368_383	

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0C4E **OTP_DOUT_384_399** **OTP dout 384 399** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_384_399															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_384_399	

0C50 **OTP_DOUT_400_415** **OTP dout 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_400_415															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_400_415	

0C52 **OTP_DOUT_416_431** **OTP dout 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_416_431															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_416_431	

0C54 **OTP_DOUT_432_447** **OTP dout 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_432_447															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_432_447	

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0C56 **OTP_DOUT_448_463** **OTP dout 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_448_463															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_448_463	

0C58 **OTP_DOUT_464_479** **OTP dout 464 479** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_464_479															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_464_479	

0C5A **OTP_DOUT_480_495** **OTP dout 480 495** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_480_495															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_480_495	

0C5C **OTP_DOUT_496_511** **OTP dout 496 511** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_496_511															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_496_511	

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0C5E **OTP_VAL_0_15** **OTP val 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_0_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_0_15	

0C60 **OTP_VAL_16_31** **OTP val 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_16_31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_16_31	

0C62 **OTP_VAL_32_47** **OTP val 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_32_47															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_32_47	

0C64 **OTP_VAL_48_63** **OTP val 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_48_63															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_48_63	

0C66 **OTP_VAL_64_79** **OTP val 64 79** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_64_79															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_64_79	

0C68 **OTP_VAL_80_95** **OTP val 80 95** **2940**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_80_95															
Type	RW															
Reset	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_80_95	

0C6A **OTP_VAL_96_111** **OTP val 96 111** **1B00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_96_111															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_96_111	

0C6C **OTP_VAL_112_127** **OTP val 112 127** **4100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_112_127															
Type	RW															
Reset	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_112_127	

0C6E **OTP_VAL_128_143** **OTP val 128 143** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_128_143															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_128_143	

0C70 OTP_VAL_144_159 OTP val 144 159 01E0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_VAL_144_159**															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_144_159	

0C72 OTP_VAL_160_175 OTP val 160 175 3600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_VAL_160_175**															
Type	RW															
Reset	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_160_175	

0C74 OTP_VAL_176_191 OTP val 176 191 0064

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_VAL_176_191**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_176_191	

0C76 OTP_VAL_192_207 OTP val 192 207 0400

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_VAL_192_207**															

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Type	RW															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_192_207	

0C78 OTP_VAL_208_223 OTP val 208 223 0800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_208_223															
Type	RW															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_208_223	

0C7A OTP_VAL_224_239 OTP val 224 239 1000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_224_239															
Type	RW															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_224_239	

0C7C OTP_VAL_240_255 OTP val 240 255 1800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_240_255															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_240_255	

0C7E OTP_VAL_256_271 OTP val 256 271 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_256_271															

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Type	RW															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_256_271	

0C80 OTP_VAL_272_287 OTP val 272 287 6000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_272_287															
Type	RW															
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_272_287	

0C82 OTP_VAL_288_303 OTP val 288 303 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_288_303															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_288_303	

0C84 OTP_VAL_304_319 OTP val 304 319 7B7B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_304_319															
Type	RW															
Reset	0	1	1	1	1	0	1	1	0	1	1	1	1	0	1	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_304_319	

0C86 OTP_VAL_320_335 OTP val 320 335 7B7B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_320_335															

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Type	RW															
Reset	0	1	1	1	1	0	1	1	0	1	1	1	1	0	1	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_320_335	

0C88 **OTP_VAL_336_351** **OTP val 336 351** **7B7B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_336_351															
Type	RW															
Reset	0	1	1	1	1	0	1	1	0	1	1	1	1	0	1	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_336_351	

0C8A **OTP_VAL_352_367** **OTP val 352 367** **007B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_352_367															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_352_367	

0C8C **OTP_VAL_368_383** **OTP val 368 383** **A000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_368_383															
Type	RW															
Reset	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_368_383	

0C8E **OTP_VAL_384_399** **OTP val 384 399** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_384_399															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_384_399	

0C90 **OTP_VAL_400_415** **OTP val 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_400_415															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_400_415	

0C92 **OTP_VAL_416_431** **OTP val 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_416_431															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_416_431	

0C94 **OTP_VAL_432_447** **OTP val 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_432_447															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_432_447	

0C96 **OTP_VAL_448_463** **OTP val 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_448_463															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_448_463	

0C98 OTP_VAL_464_479 OTP val 464 479 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_464_479															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_464_479	

0C9A OTP_VAL_480_495 OTP val 480 495 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_480_495															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_480_495	

0C9C OTP_VAL_496_511 OTP val 496 511 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_496_511															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_496_511	

0CA6 FGADC_CON1 FGADC Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_34_19															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_34_19	**Current charge value[34:19]**

0CA8 FGADC_CON2 FGADC Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_18_03															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_18_03	Current charge value[18:3]

0CAA FGADC_CON3 FGADC Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FG_CAR_02_00		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	FG_CAR_02_00	Current charge value[2:0]

0CAC FGADC_CON4 FGADC Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_32_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_32_17	Current charge time value[32:17]

0CAE FGADC_CON5 FGADC Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_16_01															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_16_01	Current charge time value[16:1]

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0CB0 FGADC_CON6 FGADC Control Register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FG_NTER_00
Type																RO
Reset																0

Bit(s)	Name	Description
0	FG_NTER_00	Current charge time value[0]

0CBA FGADC_CON11 FGADC Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	Current output charge of first stage[15:0]

0CC0 FGADC_CON14 FGADC Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_FGANALOGTEST			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_FGANALOGTEST	FGADC test bits

0CF2 AUDDEC_ANA_CON0 AUDDEC Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRSCDISABLE_VAUDP32	RG_AUDHPLSCDISABLE_VAUDP32	RG_AUDHSSCDISABLE_VAUDP32	RG_AUDHPRMUXINPUTSEL_VAUDP32		RG_AUDHPLMUXINPUTSEL_VAUDP32		RG_AUDHSMUXINPUTSEL_VAUDP32		RG_AUDHPRPWRUP_VAUDP32	RG_AUDHPLPWRUP_VAUDP32	RG_AUDHSPWRUP_VAUDP32	RG_AUDDACPWLUP_VA32	RG_AUDDACPWRUP_VA32	RG_AUDDACRPWRUP_VAUDP32	RG_AUDDACLPWRUP_VAUDP32
Type	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRSCDISABLE_VAUDP32	**Disables headphone right short circuit protection**

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Bit(s)	Name	Description
14	RG_AUDHPLSCDISABLE_VAUDP32	**Disables headphone left short circuit protection**
13	RG_AUDHSSCDISABLE_VAUDP32	**Disables headset short circuit protection**
12:11	RG_AUDHPRMUXINPUTSEL_VAUDP32	**Selects audio right headphone input multiplexor** Positive/negative pins: 00: Open/open 01: LoudSPK playback 10: Audio playback 11: Test mode
10:9	RG_AUDHPLMUXINPUTSEL_VAUDP32	**Selects audio left headphone input multiplexor Positive/negative pins:** 00: Open/open 01: LoudSPK playback 10: Audio playback 11: Test mode
8:7	RG_AUDHSMUXINPUTSEL_VAUDP32	**Selects audio handset input multiplexor** Positive/negative pins: 00: Open/open 01: MUTE (input grounded) 10: Voice playback 11: Test mode
6	RG_AUDHPRPWRUP_VAUDP32	**Powers up audio right headphone**
5	RG_AUDHPLPWRUP_VAUDP32	**Powers up audio left headphone**
4	RG_AUDHSPWRUP_VAUDP32	**Powers up audio headset**
3	RG_AUD_DAC_PWL_UP_VA32	**Power-down control for left channel audio biasgen** 0: Power down 1: Enable
2	RG_AUD_DAC_PWR_UP_VA32	**Power-down control for right channel audio biasgen** 0: Power down 1: Enable
1	RG_AUDDACRPWRUP_VAUDP32	**Power-down control for right-channel audio DAC** 0: Power down 1: Enable
0	RG_AUDDACLPWRUP_VAUDP32	**Power-down control for left-channel audio DAC** 0: Power down 1: Enable

0CF4 **AUDDEC_ANA_CON1** **AUDDEC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HPOUTPUTRESET0_VAUDP32	RG_HPINPUTRESET0_VAUDP32	RG_HPOUTPUTSTBENH_VAUDP32	RG_HPINPUTSTBENH_VAUDP32	RG_HSOUT_SHORTVCM_VAUDP32	RG_HSOUTPUTRESET0_VAUDP32	RG_HSINPUTRESET0_VAUDP32	RG_HSOUTPUTSTBENH_VAUDP32	RG_HSINPUTSTBENH_VAUDP32	RG_PRECHARGEBUF_EN_VAUDP32	RG_AUDBGBON_VAUDP32	RG_AUDHPSTARTUP_VAUDP32	RG_AUDHSSTARTUP_VAUDP32	RG_AUDHPRBSCCURRENT_VAUDP32	RG_AUDHPLBSCCURRENT_VAUDP32	RG_AUDHSBSCCURRENT_VAUDP32
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_HPOUTPUTRESETo_VAUDP32	**Resets HPL/R driver SE output to 0V ground** 0: No reset 1: Reset
14	RG_HPINPUTRESET0_VAUDP32	**Resets HP driver input to ground** 0: No reset 1: Reset
13	RG_HPOUTPUTSTBENH_VAUDP32	**HP driver output stability enhancement option** 0: No enhancement 1: Enhance
12	RG_HPINPUTSTBENH_VAUDP32	**HP driver input stability enhancement option** 0: No enhancement 1: Enhance
11	RG_HSOUT_SHORTVCM_VAUDP32	**Shorts HS output to VCM** (DCC: 0V; ACC: 1.4V) 0: Does not short to VCM 1: Short to VCM
10	RG_HSOUTPUTRESETo_VAUDP32	**Resets HS driver DE outputs to 0V ground** 0: No reset 1: Reset
9	RG_HSINPUTRESET0_VAUDP32	**Resets HS driver DE inputs to 0V ground** 0: No reset 1: Reset
8	RG_HSOUTPUTSTBENH_VAUDP32	**HS driver output stability enhancement option** 0: No enhancement 1: Enhance
7	RG_HSINPUTSTBENH_VAUDP32	**HS driver input stability enhancement option** 0: No enhancement 1: Enhance
6	RG_PRECHARGEBUF_EN_VAUDP32	**Enables pre-charge buffer stage 2** 0: Disable 1: Enable
5	RG_AUDBGBON_VAUDP32	**Modifies BG voltages in HP & Line Amps**
4	RG_AUDHPSTARTUP_VAUDP32	**Forces a Startup mode in HP Amps if required**
3	RG_AUDHSSTARTUP_VAUDP32	**Forces a Startup mode in HS Amp if required**
2	RG_AUDHPRBSCCURRENT_VAUDP32	**Audio right headphone BSC current**
1	RG_AUDHPLBSCCURRENT_VAUDP32	**Audio left headphone BSC current**
0	RG_AUDHSBSCCURRENT_VAUDP32	**Audio handset BSC current**

0CF6 **AUDDEC_ANA_CON2** **AUDDEC Control Register 2** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_AUDHPLFINETRIM_VAUDP32		RG_AUDHPTRIM_EN_VAUDP32	RG_AUDHPRTRIM_VAUDP32				RG_AUDHPLTRIM_VAUDP32				RG_LINENOISEENH_VAUDP32	RG_HPOUTSTB_RSEL_VAUDP32			RG_HPOUT_SHORTVCM_VAUDP32
Type	RW		RW	RW				RW				RW	RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:14	RG_AUDHPLFINETRIM_VAUDP32	**Fine trim offset voltage of HPL** 01: -0.5mV 10: +0.5mV
13	RG_AUDHPTRIM_EN_VAUDP32	**Enable control of trim circuit of HP** 0: Disable trim circuit 1: Enable trim circuit
12:9	RG_AUDHPRTRIM_VAUDP32	**Trim offset voltage of HPR** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
8:5	RG_AUDHPLTRIM_VAUDP32	**Trim offset voltage of HPL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
4	RG_LINENOISEENH_VAUDP32	**HP driver noise enhancement option under line-in playback** 0: No enhancement 1: Enhance
3:1	RG_HPOUTSTB_RSEL_VAUDP32	**Selects HP OUTSTB resistance** <2>=0: DCC mode <2>=1: ACC mode
0	RG_HPOUT_SHORTVCM_VAUDP32	**Shorts HP output to VCM** (DCC: 0V; ACC: 1.4V) 0: Does not short to VCM

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Bit(s)	Name	Description
		1: Short to VCM

0CF8 AUDDEC_ANA_CON3 AUDDEC Control Register 3 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_LOOUTSTB_RSEL_VAUDP32			RG_LOOUT_SHORTVCM_VAUDP32	RG_LOOUTPUTRESET0_VAUDP32	RG_LOINPUTRESET0_VAUDP32	RG_LOOUTPUTSTBENH_VAUDP32	RG_LOINPUTSTBENH_VAUDP32	RG_AUDLOSTARTUP_VAUDP32	RG_AUDLOLBSCCURRENT_VAUDP32	RG_AUDLOLSCDISABLE_VAUDP32	RG_AUDLOLMUXINPUTSEL_VAUDP32		RG_AUDLOLPWRUP_VAUDP32	RG_AUDHPRFINETRIM_VAUDP32	
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:13	RG_LOOUTSTB_RSEL_VAUDP32	**Selects LO buffer OUTSTB resistance** <2>=0: DCC mode <2>=1: ACC mode
12	RG_LOOUT_SHORTVCM_VAUDP32	**Short LO output to VCM** (DCC: 0V; ACC: 1.4V) 0: Does not short to VCM 1: Short to VCM
11	RG_LOOUTPUTRESET0_VAUDP32	**Resets LOL/R driver SE output to 0V ground** 0: No reset 1: Reset
10	RG_LOINPUTRESET0_VAUDP32	**Resets LO driver input to ground** 0: No reset 1: Reset
9	RG_LOOUTPUTSTBENH_VAUDP32	**LO driver output stability enhancement option** 0: No enhancement 1: Enhance
8	RG_LOINPUTSTBENH_VAUDP32	**LO driver input stability enhancement option** 0: No enhancement 1: Enhance
7	RG_AUDLOSTARTUP_VAUDP32	**Forces a Startup mode in LO Amps if required**
6	RG_AUDLOLBSCCURRENT_VAUDP32	**Audio left LO buffer BSC current**
5	RG_AUDLOLSCDISABLE_VAUDP32	**Disables LO buffer left short circuit protection**
4:3	RG_AUDLOLMUXINPUTSEL_VAUDP32	**Selects audio left LO buffer input multiplexor** Positive/negative pins: 00: Open/open 01: MUTE (input grounded) 10: Audio playback 11: Test mode
2	RG_AUDLOLPWRUP_VAUDP32	**Powers up audio left LO buffer**
1:0	RG_AUDHPRFINETRIM_VAUDP32	**Fine trim offset voltage of HPR** 01: -0.5mV

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Bit(s)	Name	Description
		10: +0.5mV

0CFA **AUDDEC_ANA_CON4** **AUDDEC Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDHPSPKDET_EN_VAUDP32	RG_AUDTRIMBUF_GAINSEL_VAUDP32		RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP32				RG_AUDTRIMBUF_EN_VAUDP32	RG_AUDLOLFINETRIM_VAUDP32		RG_AUDLOTRIM_EN_VAUDP32	RG_AUDLOLTRIM_VAUDP32			
Type		RW	RW		RW				RW	RW		RW	RW			
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_AUDHPSPKDET_EN_VAUDP32	**Enables audio headphone speaker detection**
13:12	RG_AUDTRIMBUF_GAINSEL_VAUDP32	**Selects audio offset trimming buffer gain** 00: 0dB 01: 6dB 10: 12dB 11: 18dB
11:8	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP32	**Selects audio offset trimming buffer mux** 0000: Open 0001: HPL 0010: HPR 0011: HSP 0100: HSN 0101: LOLP 0110: LOLN 0111: LORP 1000: LORN 1001: AVSS32 1010~1111: Unused
7	RG_AUDTRIMBUF_EN_VAUDP32	**Enables audio offset trimming buffer**
6:5	RG_AUDLOLFINETRIM_VAUDP32	**Fine trim offset voltage of LOL** 01: -0.5mV 10: +0.5mV
4	RG_AUDLOTRIM_EN_VAUDP32	**Enable control of trim circuit of LO buffer** 0: Disable trim circuit 1: Enable trim circuit
3:0	RG_AUDLOLTRIM_VAUDP32	**Trim offset voltage of LOL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV

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Bit(s)	Name	Description
		1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV

0CFC AUDDEC_ANA_CON5 AUDDEC Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_ABIDEC_RSVD0_VA32								RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP32		RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP32	
Type					RW								RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:4	RG_ABIDEC_RSVD0_VA32	**Reserves one byte in VA32 domain**
3:2	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP32	**Selects audio headphone speaker detection output mux** 00: Open 01: HPL 10: HPR 11: Unused
1:0	RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP32	**Enables audio headphone speaker detection input mux** 00: Open 01: DACLP 10: DACLN 11: DACRP

0CFE AUDDEC_ANA_CON6 AUDDEC Control Register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD0_VAUDP32								RG_ABIDEC_RSVD1_VA32							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD0_VAUDP32	Reserves one byte in VAUDP32 domain
7:0	RG_ABIDEC_RSVD1_VA32	Reserves one byte in VA32 domain

0D00 AUDDEC_ANA_CON7 AUDDEC Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name					RG_AUDZCDCLKSEL_VAUDP32	RG_AUDZCDMUXSEL_VAUDP32			RG_ABIDEC_RSVD1_VAUDP32							
Type					RW	RW			RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_AUDZCDCLKSEL_VAUDP32	**Increases ZCD comparator speed** 0: Normal speed 1: Improved speed
10:8	RG_AUDZCDMUXSEL_VAUDP32	**Selects zero crossing detection mux** 000: LOL and LOR 001: HPL and HPR 010: Handset 011: Unused 100: Bypass ZCD
7:0	RG_ABIDEC_RSVD1_VAUDP32	**Reserves one byte in VAUDP32 domain**

0D02 AUDDEC_ANA_CON8 AUDDEC Control Register 8 0092

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AUDBIASADJ_0_VAUDP32								
Type								RW								
Reset								0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
8:0	RG_AUDBIASADJ_0_VAUDP32	**Audio bias adjustment 0, bits:** [2:0] Headphone Left/Right DR bias current setting [5:3] Handset DR bias current setting. DR bias settings [8:6] Line-out DR bias current setting. DR bias settings 000: 4uA 001: 5uA 010: 6uA 011: 7uA 100: 8uA 101: 9A 110: 10uA 111: 11uA

0D04 AUDDEC_ANA_CON9 AUDDEC Control Register 9 1155

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_LCLDO_DEC_REMOTE_SENSE_	RG_LCLDO_DEC_PDDIS_EN_VA18	RG_LCLDO_DEC_EN_VA32	RG_AUDGLB_PWRDN_VA32	RG_SEL_DELAY_VCORE	RG_SEL_DECODER_96K_VA32	RG_RSTB_DECODER_VA32	RG_AUDIBIASPWRDN_VAUDP32	RG_AUDBIASADJ_1_VAUDP32							

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	VA18															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW							
Reset	0	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	RG_LCLDO_DEC_REMOTE_SENSE_VA18	**Selects LCLDO_DEC remote sense** 0: Local sense 1: Remote sense
14	RG_LCLDO_DEC_PDDIS_EN_VA18	**Enables LCLDO_DEC power-down discharge**
13	RG_LCLDO_DEC_EN_VA32	**Enables LCLDO_DEC**
12	RG_AUDGLB_PWRDN_VA32	**Power-down control for audio global bias circuit** 0: Enable 1: Disable; default on
11	RG_SEL_DELAY_VCORE	**Selects AFIFO read clock delay** 0: 5ns 1: 10ns
10	RG_SEL_DECODER_96K_VA32	**Selects audio DAC clock** 0: 6.5MHz 1: 13MHz
9	RG_RSTB_DECODER_VA32	**Resets audio decoder reset** 0: Reset 1: Normal
8	RG_AUDIBIASPWRDN_VAUDP32	**Power-down control for IbiasDistrib circuit** 0: Enable 1: Disable
7:0	RG_AUDBIASADJ_1_VAUDP32	**Audio bias adjustment 1, bits:** [7:6] ZCD bias current setting 00: 3uA 01: 4uA 10: 5uA 11: 6uA [5:4] LOL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [3:2] HS ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [1:0]: HPL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA

0D06 **AUDDEC_ANA_CON10** **AUDDEC Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDGL	RG_NVREG	RG_NVREG	RG_AUDPMU_RSVD_VA18							

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						B_LP2_VOW_EN_VA32	_PULL0V_VAUDP32	_EN_VAUDP32								
Type						RW	RW	RW	RW							
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	RG_AUDGLB_LP2_VOW_EN_VA32	**Enables AUDGLB VOW low-power mode** OP and self-bias will be down and IREF from PMU_TOP.
9	RG_NVREG_PULL0V_VAUDP32	**NVREG output pulled to 0V when PD**
8	RG_NVREG_EN_VAUDP32	**Enables NVREG**
7:0	RG_AUDPMU_RSVD_VA18	**Reserves 1 byte for VA18 domain**

0D08 **AUDENC_ANA_CON0** **AUDENC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP		RG_AUDPREAMPLGAIN			RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCPRECHARGE	RG_AUDPREAMPLDCCEN	RG_AUDPREAMPLON
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCLINPUTSEL	**Selects audio L ADC input** 00: Idle 01: AIN0 10: Left preamplifier 11: Idle
12	RG_AUDADCLPWRUP	**Powers up audio L ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPLGAIN	**Adjusts audio L preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPLVSCALE	**Audio L preamplifier PGA DC output voltage scale**
5:4	RG_AUDPREAMPLINPUTSEL	**Selects audio L preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
3	RG_AUDPREAMPLP	**Enables audio L preamplifier PGA test**

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Bit(s)	Name	Description
	GATEST	0: Disable 1: Enable
2	RG_AUDPREAMPLDCPRECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPLDCCEN	**Audio L DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPLON	**Enables audio L preamplifier** 0: Disable 1: Enable

0D0A **AUDENC_ANA_CON1** **AUDENC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCRINPUTSEL		RG_AUDADCRPWRUP		RG_AUDPREAMPRGAIN			RG_AUDPREAMPRVSCALE		RG_AUDPREAMPRINPUTSEL		RG_AUDPREAMPRPGATEST	RG_AUDPREAMPRDCPRECHARGE	RG_AUDPREAMPRDCCEN	RG_AUDPREAMPRON
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCRINPUTSEL	**Selects audio R ADC input** 00: Idle 01: AIN0 10: Right preamplifier 11: Idle
12	RG_AUDADCRPWRUP	**Powers up audio R ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPRGAIN	**Adjusts audio R preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPRVSCALE	**Audio R preamplifier PGA DC output voltage scale**
5:4	RG_AUDPREAMPRINPUTSEL	**Selects audio R preamplifier input** 00: None 01: AIN0 10: AIN3 11: AIN2
3	RG_AUDPREAMPRPGATEST	**Enables audio R preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPRDCPRECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0: Disable

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Bit(s)	Name	Description
		1: Enable
1	RG_AUDPREAMPRDCCEN	**Audio R DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPRON	**Enables audio R preamplifier** 0: Disable 1: Enable

0D0C **AUDENC_ANA_CON2** **AUDENC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCFLASHIDDTEST		RG_AUDADCREFBUFIDDTEST		RG_AUDADC2NDSTAGEIDDTEST		RG_AUDADC1STSTAGEIDDTEST		RG_AUDPREAMPIDDTEST		RG_AUDADCFLASHLPEN	RG_AUDADC2NDSTAGELPEN	RG_AUDADC1STSTAGELPEN	RG_AUDPREAMPLPEN	RG_AUDGLBVOWLPWEN	RG_AUDULHALFBIAS
Type	RW		RW		RW		RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Selects audio ADC flash Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Selects audio ADC reference buffer Idd current** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Audio ADC 2nd and 3rd stage Idd adjustment bits** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Audio ADC 1st stage Idd adjustment bits** 00: 100% 01: 80% 10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Audio preamplifier Idd adjustment bits** 00: 100% 01: 75% 10: 125% 11: 150%
5	RG_AUDADCFLASHLPEN	**Enables audio ADC flash low power** 0: Normal 1: Enable
4	RG_AUDADC2NDSTAGELPEN	**Enables audio ADC 2nd and 3rd low power** 0: Normal 1: Enable

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Bit(s)	Name	Description
3	RG_AUDADC1STSTAGELPEN	**Enables audio ADC 1st stage low power** 0: Normal 1: Enable
2	RG_AUDPREAMPLPEN	**Audio preamplifier PGA low power mode** 0: Disable 1: Enable
1	RG_AUDGLBVOWLPWEN	**Enables audio uplink globe bias VOW low power mode** 0: Normal 1: Enable
0	RG_AUDULHALFBIAS	**Enables audio uplink halfbias** 0: Normal 1: Enable

0D0E **AUDENC_ANA_CON3** **AUDENC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREPGA					RG_DCCVCMBUFLPSWEN	RG_DCCVCMBUFLPMODSEL	RG_AUDPREAMPAAFEN		RG_AUDADCCLKRSTB	RG_AUDADCCLKGENMODE		RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL	RG_AUDADCDACoP25FS
Type	RW					RW	RW	RW		RW	RW		RW		RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
15:11	RG_AUDSPAREPGA	**Spare control bits for PGA**
10	RG_DCCVCMBUFLPSWEN	**Audio preamplifier PGA DCC VCM buffer SW EN**
9	RG_DCCVCMBUFLPMODSEL	**Audio preamplifier PGA DCC VCM buffer LP MODSEL**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0: Disable 1: Enable
6	RG_AUDADCCLKRSTB	**Audio ADC clock RSTB** 0: Reset 1: Enable
5:4	RG_AUDADCCLKGENMODE	**Audio ADC clock gen. mode** 00: Divided by 2 (normal) 01: Divided by 4 10: Divided by 8 11: Not divided
3:2	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00: 13MHz from CLKSQ 01: 3.25MHz from CLKSQ 10: 12.58MHz from 32kHz PLL 11: 12MHz ring oscillator
1	RG_AUDADCCLKSEL	**Selects audio ADC clock** 0: 13MHz clock in, 6.5MHz data out 1: 26MHz clock in, 13MHz data out
0	RG_AUDADCDACoP2	**Enables audio ADC FBDAC 0.25FS**

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Bit(s)	Name	Description
	5FS	0: 13MHz clock in, 6.5MHz data out 1: 3.25MHz clock in, 1.625MHz data out

0D10 AUDENC_ANA_CON4 AUDENC Control Register 4 0800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDADCDACTEST	RG_AUDADCNODEM	RG_AUDADCDACNRZ	RG_AUDADCDACIDDTEST		RG_AUDADCDACFBCURRENT	RG_AUDADCFFBYPASS	RG_AUDADCBYPASS	RG_AUDADCNOPATEST	RG_AUDADCWIDECM	RG_AUDADCFSRESET	RG_AUDADC3RDSTAGERESET	RG_AUDADC2NDSTAGERESET	RG_AUDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0: Disable 1: Enable data in RG_AUDADCTESTDATA[15:0] to be passed to DAC.
12	RG_AUDADCNODEM	**Audio ADC DEM test**
11	RG_AUDADCDACNRZ	**Audio ADC DAC in non return to zero mode** 0: RZ mode (2I) 1: NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Selects audio ADC-DAC Idd current test** 00: Normal 11: -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBYPASS	**Bypasses audio ADC feedforward** 0: No bypass. Allow feedforward coefficient to pass signal to ADC flash. 1: Bypass. Does not allow ADC i/p signal to feedforward flash.
6	RG_AUDADCBYPASS	**Enables audio ADC input resistor bypass** 0: Disable 1: Enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0: Normal ADC gain 1: 6dB ADC gain
4	RG_AUDADCWIDECM	**Enables audio ADC wide common mode** 0: Normal 1: Enable
3	RG_AUDADCFSRESET	**Selects audio encoder FS reset block model**
2	RG_AUDADC3RDSTAGERESET	**Audio ADC 3rd stage reset** 0: Normal 1: Reset
1	RG_AUDADC2NDSTAGERESET	**Audio ADC 2nd stage reset** 0: Normal 1: Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0: Enable

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Bit(s)	Name	Description
		1: Disable

0D12 AUDENC_ANA_CON5 AUDENC Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCTESTDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_AUDADCTESTDATA	**Audio ADC test data bits** Audio ADC test data bits for both phases of DRTZ DAC. Can enable any current source you choose.

0D14 AUDENC_ANA_CON6 AUDENC Control Register 6 1515

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL	RG_AUDRCTUNER							RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW	RW							RW	RW				
Reset			0	1	0	1	0	1			0	1	0	1	0	1

Bit(s)	Name	Description
13	RG_AUDRCTUNERSEL	**Selects audio R ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
12:8	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE.
5	RG_AUDRCTUNELSEL	**Selects audio L ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE.

0D16 AUDENC_ANA_CON7 AUDENC Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVA18								RG_AUDSPAREVA30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:8	RG_AUDSPAREVA18	Spare control bits for AVDD18 voltage domain
7:0	RG_AUDSPAREVA30	Spare control bits for AVDD30 voltage domain

0D18 AUDENC_ANA_CON8 AUDENC Control Register 8 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:9	RG_DMICMONSEL	**Enables digital microphone monitor path**
8	RG_DMICMONEN	**Enables digital microphone monitor path** 0: Disable 1: Enable (26MHz)
7:6	RG_AUDDIGMICNDUTY	**Digital microphone negative duty control**
5:4	RG_AUDDIGMICPDUTY	**Digital microphone positive duty control**
3	RG_DMICHPCLKEN	**Enables digital microphone monitor path selection** 0: DCC CLK 1: CLKSQ
2:1	RG_AUDDIGMICBIAS	**Digital microphone slew rate control** 11>10>01>00
0	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

0D1A AUDENC_ANA_CON9 AUDENC Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDMICBIAS2LOWPEN	RG_AUDMICBIAS2VREF			RG_AUDMICBIAS2DCSW2NEN	RG_AUDMICBIAS2DCSW2P2EN	RG_AUDMICBIAS2DCSW2P1EN	RG_AUDPWDBMICBIAS2	RG_AUDMICBIAS0LOWPEN	RG_AUDMICBIAS0VREF			RG_AUDMICBIAS0DCSW0NEN	RG_AUDMICBIAS0DCSW0P2EN	RG_AUDMICBIAS0DCSW0P1EN	RG_AUDPWDBMICBIAS0
Type	RW	RW			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDMICBIAS2LOWPEN	**Enables MIC Bias 2 low power** 0: High power mode 1: Low power mode

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Bit(s)	Name	Description
14:12	RG_AUDMICBIAS2VREF	**Selects MIC Bias 2 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: 2.6V 111: 2.7V
11	RG_AUDMICBIAS2DCSW2NEN	**MIC Bias 2 DC couple switch 2N** 0: Off 1: On
10	RG_AUDMICBIAS2DCSW2P2EN	**MIC Bias 2 DC couple switch 2P2** 0: Off 1: On
9	RG_AUDMICBIAS2DCSW2P1EN	**MIC Bias 2 DC couple switch 2P1** 0: Off 1: On
8	RG_AUDPWDBMICBIAS2	**Powers down MIC Bias 2** 0: Power down 1: Power on
7	RG_AUDMICBIAS0LOWPEN	**Enables MIC Bias 0 low power** 0: High power mode 1: Low power mode
6:4	RG_AUDMICBIAS0VREF	**Selects MIC Bias 0 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: 2.6V 111: 2.7V
3	RG_AUDMICBIAS0DCSW0NEN	**MIC Bias 0 DC couple switch 0N** 0: Off 1: On
2	RG_AUDMICBIAS0DCSW0P2EN	**MIC Bias 0 DC couple switch 0P2** 0: Off 1: On
1	RG_AUDMICBIAS0DCSW0P1EN	**MIC Bias 0 DC couple switch 0P1** 0: Off 1: On
0	RG_AUDPWDBMICBIAS0	**Powers down MIC Bias 0** 0: Power down 1: Power on

0D1C **AUDENC_ANA_CON10** **AUDENC Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_BANDGAPG	RG_AUDMICBIA	RG_AUDMICBIA	RG_AUDMICBIA	RG_AUDMICBIA	RG_AUDMICBIA	RG_AUDMICBIAS1VREF				RG_AUDMICBIA	RG_AUDMICBIA	RG_AUDPWDB

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				EN	S2DC SW3 NEN	S2DC SW3P EN	S1DC SW3 NEN	S1DC SW3P EN	S1LO WPE N					S1DC SW1N EN	S1DC SW1P EN	MICB IAS1
Type				RW	RW	RW	RW	RW	RW	RW				RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
12	RG_BANDGAPGEN	**Remote sense to bandgap ground** 0: Disable 1: Enable
11	RG_AUDMICBIAS2DCSW3NEN	**MIC Bias 2 DC couple switch 3N** 0: Off 1: On
10	RG_AUDMICBIAS2DCSW3PEN	**MIC Bias 2 DC couple switch 3P** 0: Off 1: On
9	RG_AUDMICBIAS1DCSW3NEN	**MIC Bias 1 DC couple switch 3N** 0: Off 1: On
8	RG_AUDMICBIAS1DCSW3PEN	**MIC Bias 1 DC couple switch 3P** 0: Off 1: On
7	RG_AUDMICBIAS1LOWPEN	**Enables MIC Bias 1 low power** 0: High power mode 1: Low power mode
6:4	RG_AUDMICBIAS1VREF	**Selects MIC Bias 1 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: 2.6V 111: 2.7V
2	RG_AUDMICBIAS1DCSW1NEN	**MIC Bias 1 DC couple switch 1N** 0: Off 1: On
1	RG_AUDMICBIAS1DCSW1PEN	**MIC Bias 1 DC couple switch 1P** 0: Off 1: On
0	RG_AUDPWDBMICBIAS1	**Powers down MIC Bias 1** 0: Power down 1: Power on

0D1E **AUDENC_ANA_CON11** **AUDENC Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ NVC MPS WEN	RG_N VMO DSEL	RG_N VDET VTH	RG_N VDET CMPE N	RG_E INTC ONFI GACC DET	RG_E INTC OMP VTH	RG_S WBU FSWE N	RG_S WBU FMO DSEL	RG_A CCDE T2SE L	RG_A CCDE T1SE L	RG_A UDAC CDET VTHB CAL	RG_A UDAC CDET VTHA CAL	RG_A UDAC CDET VIN1 PULL LOW	RG_A UDAC CDET MICB IAS2 PULL	RG_A UDAC CDET MICB IAS1P ULLL	RG_A UDA CCDE TMIC BIAS 0PUL

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														LOW	OW	LLO W
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_NVCMPSWEN	**SW mode control for NV detector** 0: Power down 1: Power on
14	RG_NVMODSEL	**NV detector control mode** 0: Hardware mode 1: Software mode
13	RG_NVDETVTH	**Voltage threshold of detecting negative voltage**
12	RG_NVDETCMPEN	**Enables negative voltage detection** 0: Disable 1: Enable
11	RG_EINTCONFIGACCDET	**Internal connection between ACCDET and EINT** 0: Disable 1: Enable (EINT connected with ACCDET pin and ACCDETSEL should be 1.)
10	RG_EINTCOMPVTH	**EINT comparator threshold** 0: 6/8 => 2.4V 1: 5/8 => 2V
9	RG_SWBUFSWEN	**Switch buffer turns on SW mode control for ACCDET to AUXADC** 0: Power down 1: Power on
8	RG_SWBUFMODSEL	**Controls buffer power** 0: Hardware mode 1: Software mode
7	RG_ACCDET2SEL	**Selects ACCDET2 input** 0: ACCDET 2 1: MIC3P pin
6	RG_ACCDET1SEL	**Selects ACCDET1 input** 0: ACCDET1 1: MIC1P pin
5	RG_AUDACCDETVTHBCAL	**Calibrates audio accessory detection voltage threshold B**
4	RG_AUDACCDETVTHACAL	**Calibrates audio accessory detection voltage threshold A**
3	RG_AUDACCDETVIN1PULLLOW	**Pulls low VIN1 pads when MICBIAS is off** 0: Disable 1: Enable
2	RG_AUDACCDETMICBIAS2PULLLOW	**Pulls low MIC Bias 2 pads when MICBIAS is off** 0: Disable 1: Enable
1	RG_AUDACCDETMICBIAS1PULLLOW	**Pulls low MIC Bias 1 pads when MICBIAS is off** 0: Disable 1: Enable
0	RG_AUDACCDETMICBIAS0PULLLOW	**Pulls low MIC Bias 0 pads when MICBIAS is off** 0: Disable 1: Enable

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0D20 AUDENC_ANA_CON12 AUDENC Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDENCSPAREVA18								RG_AUDENCSPAREVA30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_AUDENCSPAREVA18	Spare control bits for AVDD18 voltage domain
7:0	RG_AUDENCSPAREVA30	Spare control bits for AVDD30 voltage domain

0D22 AUDENC_ANA_CON13 AUDENC Control Register 13 0310

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_PDIV1				RG_PLL_PDIV1_EN	RG_PLL_RLATCH_EN	RG_PLL_DIV1						RG_PLL_DCKO_SEL		RG_PLLBS_RST	RG_PLL_EN
Type	RW				RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:12	RG_PLL_PDIV1	**Div. no of post div** Divider for FGADC. Ratio = (N+2)*2
11	RG_PLL_PDIV1_EN	**post-div1: Enable** Divider for FGADC
10	RG_PLL_RLATCH_EN	**Enables fbdiv relatch** 0: Disable 1: Enable
9:4	RG_PLL_DIV1	**Div. no of fbk divider** Ratio = (N+2)*16
3:2	RG_PLL_DCKO_SEL	**Reserved**
1	RG_PLLBS_RST	**Enables PLL reset** 1'b0: Disable 1'b1: Enable
0	RG_PLL_EN	**Enables PLL CLK** 0: Disable 1: enable

0D24 AUDENC_ANA_CON14 AUDENC Control Register 14 0180

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_DCHP_EN	RG_PLL_HPM_EN	RG_PLL_CKT_EN	RG_PLL_VCT_EN	RG_PLL_CKT_SEL		RG_PLL_IBSEL		RG_CKO_SEL		RG_PLL_BR		RG_PLL_BP		RG_PLL_BC	

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Type	RW	RW	RW	RW	RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_PLL_DCHP_EN	**Reserved**
14	RG_PLL_HPM_EN	**Reserved**
13	RG_PLL_CKT_EN	**Enables clock test mode** 0: Disable 1: Enable
12	RG_PLL_VCT_EN	**Enables v-control test mode** 0: Disable 1: Enable
11:10	RG_PLL_CKT_SEL	**Selects CK test mode** 00: CKI_RTC 01: 32k from PLL 10: 406kHz 11: CK_VCO
9:8	RG_PLL_IBSEL	**Selects PLL bias current** 00: 0.5u 01: 1.0u 10: 1.5u 11: 2.0u
7:6	RG_CKO_SEL	**Selects CKO to FGADC** 00: RTC 01: 32k from PLL 10: 406kHz 11: XX
5:4	RG_PLL_BR	**Adjusts P-path resistance** 00: 800kohm 01: 400kohm 10: 150kohm 11: 150kohm
3:2	RG_PLL_BP	**Adjusts P-path capacitance** 00: 6pF 01: 8pF 10: 10pF 11: 12pF
1:0	RG_PLL_BC	**Adjusts I-path capacitance** 00: 15pF 01: 20pF 10: 25pF 11: 30pF

0D26 AUDENC_ANA_CON15 AUDENC Control Register 15 0013

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_PLL_RSVA**								**RG_PLL_DCHP_AEN**	**RG_CKDRV_EN**	**RG_VCOBAND**			**RG_PLL_CDIV**		
Type	RW								RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

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Bit(s)	Name	Description
15:8	RG_PLL_RSVA	**Reserved**
7	RG_PLL_DCHP_AEN	**Reserved**
6	RG_CKDRV_EN	**Enables clock test mode** 0: Disable 1: Enable
5:3	RG_VCOBAND	**Selects manual PLL band** 000: R-band = 16k 001: R-band = 4k 010: R-band = 8k 100: R-band = 12k
2:0	RG_PLL_CDIV	**Time domain cap multiplication ratio** 000: X1 001: X2 011: X4 111: X8

0D28 **AUDENC_ANA_CON16** **AUDENC Control Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_AUDRCTUNERREAD								RGS_AUDRCTUNELREAD				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
12:8	RGS_AUDRCTUNERREAD	Audio R RC tune read data
4:0	RGS_AUDRCTUNELREAD	Audio L RC tune read data

0D2A **AUDNCP_CLKDIV_CON0** **AUDNCP_CLKDIV Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_CHG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_CHG	

0D2C **AUDNCP_CLKDIV_CON1** **AUDNCP_CLKDIV Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name																RG_DIVCKS_ON
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_ON	

0D2E **AUDNCP_CLKDIV_CON2** **AUDNCP_CLKDIV Control Register 2** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_DIVCKS_PRG								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
8:0	RG_DIVCKS_PRG	

0D30 **AUDNCP_CLKDIV_CON3** **AUDNCP_CLKDIV Control Register 3** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_PWD_NCP
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_DIVCKS_PWD_NCP	

0D32 **AUDNCP_CLKDIV_CON4** **AUDNCP_CLKDIV Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_DIVCKS_PWD_NCP_ST_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_DIVCKS_PWD_NCP_ST_SEL	

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0E00 **AUXADC_ADC_0** **AUXADC ADC Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0	AUXADC_ADC_OUT_CH0														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

0E02 **AUXADC_ADC_1** **AUXADC ADC Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

0E04 **AUXADC_ADC_2** **AUXADC ADC Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH2				AUXADC_ADC_OUT_CH2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY	**AUXADC channel 2 output data ready**

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Bit(s)	Name	Description
	_CH2	0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

0E06 **AUXADC_ADC_3** **AUXADC ADC Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

0E08 **AUXADC_ADC_4** **AUXADC ADC Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

0E0A **AUXADC_ADC_5** **AUXADC ADC Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_				AUXADC_ADC_OUT_CH5											

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	CH5															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

0E0C **AUXADC_ADC6** **AUXADC ADC Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH6				AUXADC_ADC_OUT_CH6											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

0E0E **AUXADC_ADC7** **AUXADC ADC Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

0E10 **AUXADC_ADC** **AUXADC ADC Register 8** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ ADC_ RDY_ CH8				AUXADC_ADC_OUT_CH8											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

0E12 AUXADC_ADC9 AUXADC ADC Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ ADC_ RDY_ CH9				AUXADC_ADC_OUT_CH9											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

0E14 AUXADC_ADC10 AUXADC ADC Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ ADC_ RDY_ CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT	**AUXADC channel 10 output data**

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Bit(s)	Name	Description
	_CH10	

0E16 AUXADC_ADC_11 AUXADC ADC Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data**

0E18 AUXADC_ADC_12 AUXADC ADC Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15				AUXADC_ADC_OUT_CH12_15											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

0E1A AUXADC_ADC_13 AUXADC ADC Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_THR_HW				AUXADC_ADC_OUT_THR_HW											
Type	RO				RO											

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Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

0E1C **AUXADC_ADC_14** **AUXADC ADC Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT				AUXADC_ADC_OUT_LBAT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

0E1E **AUXADC_ADC_15** **AUXADC ADC Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT2				AUXADC_ADC_OUT_LBAT2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT2	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT2	**AUXADC low battery output data**

0E20 **AUXADC_ADC_16** **AUXADC ADC Register 16** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_GPS	AUXADC_ADC_OUT_CH7_BY_GPS														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

0E22 **AUXADC_ADC_17** **AUXADC ADC Register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_MD	AUXADC_ADC_OUT_CH7_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

0E24 **AUXADC_ADC_18** **AUXADC ADC Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_AP	AUXADC_ADC_OUT_CH7_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY	**AUXADC channel 7 output data ready**

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Bit(s)	Name	Description
	_CH7_BY_AP	0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

0E26 **AUXADC_ADC_19** **AUXADC ADC Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_MD				AUXADC_ADC_OUT_CH4_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

0E28 **AUXADC_ADC_20** **AUXADC ADC Register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

0E2A **AUXADC_ADC_21** **AUXADC ADC Register 21** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

0E2C **AUXADC_ADC_22** **AUXADC ADC Register 22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_MD	AUXADC_ADC_OUT_CH0_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

0E2E **AUXADC_ADC_23** **AUXADC ADC Register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

0E30 **AUXADC_ADC_24** **AUXADC ADC Register 24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

0E32 **AUXADC_ADC_25** **AUXADC ADC Register 25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

0E34 **AUXADC_ADC_26** **AUXADC ADC Register 26** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_VISMPS0				AUXADC_ADC_OUT_VISMPS0											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_VISMPS0	**AUXADC vismps output data ready** 0: AUXADC vismps data proceeding 1: AUXADC vismps data ready
11:0	AUXADC_ADC_OUT_VISMPS0	**AUXADC vismps output data**

0E36 AUXADC_ADC27 AUXADC ADC Register 27 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC1	AUXADC_ADC_OUT_FGADC1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC1	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC1	**AUXADC output data**

0E38 AUXADC_ADC28 AUXADC ADC Register 28 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC2	AUXADC_ADC_OUT_FGADC2														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC2	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_FGADC2	**AUXADC output data**

0E3A **AUXADC_ADC_29** **AUXADC ADC Register 29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP	AUXADC_ADC_OUT_IMP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

0E3C **AUXADC_ADC_30** **AUXADC ADC Register 30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP_AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

0E3E **AUXADC_ADC_31** **AUXADC ADC Register 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	**AUXADC channel output raw data**

0E40 **AUXADC_ADC32** **AUXADC ADC Register 32** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDRT	AUXADC_ADC_OUT_MDRT														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDRT	**AUXADC output data**

0E42 **AUXADC_ADC33** **AUXADC ADC Register 33** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDBG	AUXADC_ADC_OUT_MDBG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDBG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDBG	**AUXADC output data**

0E44 **AUXADC_ADC34** **AUXADC ADC Register 34** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_				AUXADC_ADC_OUT_JEITA											

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	JEITA															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_JEITA	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_JEITA	**AUXADC output data**

0E46 **AUXADC_ADC35** **AUXADC ADC Register 35** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_GPS				AUXADC_ADC_OUT_DCXO_BY_GPS											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_GPS	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_GPS	**AUXADC channel 4 output data**

0E48 **AUXADC_ADC36** **AUXADC ADC Register 36** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_MD				AUXADC_ADC_OUT_DCXO_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_MD	**AUXADC channel 4 output data**

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0E4A **AUXADC_ADC_37** **AUXADC ADC Register 37** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_AP				AUXADC_ADC_OUT_DCXO_BY_AP											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_AP	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_AP	**AUXADC channel 4 output data**

0E4C **AUXADC_ADC_38** **AUXADC ADC Register 38** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_MDRT				AUXADC_ADC_OUT_DCXO_MDRT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_MDRT	**AUXADC output data**

0E4E **AUXADC_ADC_39** **AUXADC ADC Register 39** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_NAG	AUXADC_ADC_OUT_NAG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_NAG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_NAG	**AUXADC output data**

0E50 **AUXADC_BUF0** AUXADC_BUF0 **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_00	AUXADC_BUF_OUT_00														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_00	**AUXADC_BUF_00** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_00	

0E52 **AUXADC_BUF1** AUXADC_BUF1 **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_01	AUXADC_BUF_OUT_01														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_01	**AUXADC_BUF_01** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_01	

0E54 **AUXADC_BUF2** AUXADC_BUF2 **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX	AUXADC_BUF_OUT_02														

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	ADC_ BUF_ RDY_ 02															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_02	**AUXADC_BUF_02** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_02	

0E56 AUXADC_BUF3 AUXADC_BUF3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 03	AUXADC_BUF_OUT_03														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_03	**AUXADC_BUF_03** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_03	

0E58 AUXADC_BUF4 AUXADC_BUF4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 04	AUXADC_BUF_OUT_04														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_04	**AUXADC_BUF_04** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_04	

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0E5A **AUXADC_BUF5** **AUXADC_BUF5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_05	AUXADC_BUF_OUT_05														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_05	**AUXADC_BUF_05** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_05	

0E5C **AUXADC_BUF6** **AUXADC_BUF6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_06	AUXADC_BUF_OUT_06														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_06	**AUXADC_BUF_06** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_06	

0E5E **AUXADC_BUF7** **AUXADC_BUF7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_07	AUXADC_BUF_OUT_07														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_07	**AUXADC_BUF_07** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_07	

0E60 **AUXADC_BUF8** **AUXADC_BUF8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_08	AUXADC_BUF_OUT_08														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_08	**AUXADC_BUF_08** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_08	

0E62 **AUXADC_BUF9** **AUXADC_BUF9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_09	AUXADC_BUF_OUT_09														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_09	**AUXADC_BUF_09** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_09	

0E64 **AUXADC_BUF10** **AUXADC_BUF10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_10	AUXADC_BUF_OUT_10														
Type	RO	RO														

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_10	**AUXADC_BUF_10** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_10	

0E66 AUXADC_BUF11 AUXADC_BUF11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_11	AUXADC_BUF_OUT_11														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_11	**AUXADC_BUF_11** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_11	

0E68 AUXADC_BUF12 AUXADC_BUF12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_12	AUXADC_BUF_OUT_12														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_12	**AUXADC_BUF_12** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_12	

0E6A AUXADC_BUF13 AUXADC_BUF13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AUX ADC_ BUF_ RDY_ 13	AUXADC_BUF_OUT_13														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_13	**AUXADC_BUF_13** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_13	

0E6C **AUXADC_BUF14** **AUXADC_BUF14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 14	AUXADC_BUF_OUT_14														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_14	**AUXADC_BUF_14** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_14	

0E6E **AUXADC_BUF15** **AUXADC_BUF15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 15	AUXADC_BUF_OUT_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_15	**AUXADC_BUF_15** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_15	

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0E70 **AUXADC_BUF16** **AUXADC_BUF16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_16	AUXADC_BUF_OUT_16														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_16	**AUXADC_BUF_16** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_16	

0E72 **AUXADC_BUF17** **AUXADC_BUF17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_17	AUXADC_BUF_OUT_17														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_17	**AUXADC_BUF_17** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_17	

0E74 **AUXADC_BUF18** **AUXADC_BUF18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_18	AUXADC_BUF_OUT_18														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_	**AUXADC_BUF_18**

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Bit(s)	Name	Description
	18	0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_18	

0E76 **AUXADC_BUF19** **AUXADC_BUF19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_19**	**AUXADC_BUF_OUT_19**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_19	**AUXADC_BUF_19** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_19	

0E78 **AUXADC_BUF20** **AUXADC_BUF20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_20**	**AUXADC_BUF_OUT_20**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_20	**AUXADC_BUF_20** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_20	

0E7A **AUXADC_BUF21** **AUXADC_BUF21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_**	**AUXADC_BUF_OUT_21**														

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	21															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_21	**AUXADC_BUF_21** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_21	

0E7C **AUXADC_BUF22** **AUXADC_BUF22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_22	AUXADC_BUF_OUT_22														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_22	**AUXADC_BUF_22** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_22	

0E7E **AUXADC_BUF23** **AUXADC_BUF23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_23	AUXADC_BUF_OUT_23														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_23	**AUXADC_BUF_23** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_23	

0E80 **AUXADC_BUF** **AUXADC_BUF24** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_24	AUXADC_BUF_OUT_24														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_24	**AUXADC_BUF_24** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_24	

0E82 **AUXADC_BUF25** **AUXADC_BUF25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_25	AUXADC_BUF_OUT_25														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_25	**AUXADC_BUF_25** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_25	

0E84 **AUXADC_BUF26** **AUXADC_BUF26** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_26	AUXADC_BUF_OUT_26														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_26	**AUXADC_BUF_26** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT	

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Bit(s)	Name	Description
	_26	

0E86 **AUXADC_BUF_27** **AUXADC_BUF27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_27	AUXADC_BUF_OUT_27														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_27	**AUXADC_BUF_27** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_27	

0E88 **AUXADC_BUF_28** **AUXADC_BUF28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_28	AUXADC_BUF_OUT_28														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_28	**AUXADC_BUF_28** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_28	

0E8A **AUXADC_BUF_29** **AUXADC_BUF29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_29	AUXADC_BUF_OUT_29														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_29	**AUXADC_BUF_29** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_29	

0E8C **AUXADC_BUF30** **AUXADC_BUF30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_30**	**AUXADC_BUF_OUT_30**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_30	**AUXADC_BUF_30** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_30	

0E8E **AUXADC_BUF31** **AUXADC_BUF31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_31**	**AUXADC_BUF_OUT_31**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_31	**AUXADC_BUF_31** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_31	

0E90 **AUXADC_STA0** **AUXADC_STA0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUX**	**AUXA**	**AUXA**	**AUXA**	**AUXADC_ADC_BUSY_IN**											

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	ADC_ADC_BUSY_IN_WAKEUP	DC_ADC_BUSY_IN_VISMPS0	DC_ADC_BUSY_IN_LBAT2	DC_ADC_BUSY_IN_LBAT												
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 0: Idle 1: Busy
14	AUXADC_ADC_BUSY_IN_VISMPS0	**ADC busy status** 0: Idle 1: Busy
13	AUXADC_ADC_BUSY_IN_LBAT2	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 0: Idle 1: Busy
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC busy status** bit[11] = CH11 ~ bit[0] = CH0 0: Idle 1: Busy

0E92 **AUXADC_STA1** **AUXADC_STA1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD	AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC2	AUXADC_ADC_BUSY_IN_FGADC1	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE	AUXADC_ADC_BUSY_IN_MDBG	AUXADC_ADC_BUSY_IN_MDRT	AUXADC_ADC_BUSY_IN_JEITA	AUXADC_ADC_BUSY_IN_DCXO_GPS	AUXADC_ADC_BUSY_IN_DCXO_GPS_MD	AUXADC_ADC_BUSY_IN_DCXO_GPS_AP	AUXADC_ADC_BUSY_IN_DCXO_MDRT
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 0: Idle 1: Busy
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 0: Idle 1: Busy
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 0: Idle

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Bit(s)	Name	Description
		1: Busy
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 0: Idle 1: Busy
10	AUXADC_ADC_BUSY_IN_FGADC2	**ADC busy status** 0: Idle 1: Busy
9	AUXADC_ADC_BUSY_IN_FGADC1	**ADC busy status** 0: Idle 1: Busy
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 0: Idle 1: Busy
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 0: Idle 1: Busy
6	AUXADC_ADC_BUSY_IN_MDBG	**ADC busy status** 0: Idle 1: Busy
5	AUXADC_ADC_BUSY_IN_MDRT	**ADC busy status** 0: Idle 1: Busy
4	AUXADC_ADC_BUSY_IN_JEITA	**ADC busy status** 0: Idle 1: Busy
3	AUXADC_ADC_BUSY_IN_DCXO_GPS	**ADC busy status** 0: Idle 1: Busy
2	AUXADC_ADC_BUSY_IN_DCXO_GPS_MD	**ADC busy status** 0: Idle 1: Busy
1	AUXADC_ADC_BUSY_IN_DCXO_GPS_AP	**ADC busy status** 0: Idle 1: Busy
0	AUXADC_ADC_BUSY_IN_DCXO_MDRT	**ADC busy status** 0: Idle 1: Busy

0E94 **AUXADC_STA2** **AUXADC_STA2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_BUSY_IN_NAG**															
Type	RO															
Reset	0															

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Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_NAG	**ADC busy status** 0: Idle 1: Busy

0F46 ACCDET_CON0 ACCDET control register 0 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUDACCDETAUXADCSWCTRL_SEL			RG_AUDACCDETTVDET		RG_AUDACCDETSWCTRL			RG_ACCDETSEL	RG_AUDACCDETANASWCTRLENB		AD_AUDACCDETCMPOC
Type					RW			RW		RW			RW	RW		RO
Reset					0			0		0	0	1	0	0		0

Bit(s)	Name	Description
11	AUDACCDETAUXADCSWCTRL_SEL	1'b0: HW mode 1'b1: SW mode
8	RG_AUDACCDETTVDET	**Puts audio accessory detection into TV mode**
6:4	RG_AUDACCDETSWCTRL	**Controls ACCDET to AUXADC switch** 001: Normal mode 010: 200K 100: 100K Others: Not allowed
3	RG_ACCDETSEL	**Selects ACCDET input** 1'b0: ACCDET pin 1'b1: MICP pin
2	RG_AUDACCDETANASWCTRLENB	
0	AD_AUDACCDETCMPOC	**ACCDET comparator_c out**

0F48 ACCDET_CON1 ACCDET Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										accdet_anaswctrl_sel	ACCDET_NEGVDET_EN_CTRL	ACCDET_NEGVDET_EN	ACCDET_EINT_SEQ_INIT	ACCDET_EINTDET_EN	ACCDET_SEQ_INIT	ACCDET_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	accdet_anaswctrl_sel	**Selects AUXADC or ACCDET controls the connection when in hook-key status**

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Bit(s)	Name	Description
		1'b0: AUXADC 1'b1: ACCDET
5	ACCDET_NEGVDET_EN_CTRL	**Initializes status default value** 1'b0: HW mode 1'b1: SW mode
4	ACCDET_NEGVDET_EN	**Enables negative debounce** 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT_SEQ_INIT	**Initializes EINT status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINTDET_EN	**Enables EINT detection** 1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**Initializes ACCDET status default value** 1'b0: Normal mode 1'b1: Initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switching to TV mode 1'b0: Disable 1'b1: Enable

0F4A **ACCDET_CON2** **ACCDET control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**ACCDET_EINT_PWM_EN**	**ACCDET_MBIAS_PWM_EN**	**ACCDET_VTH_PWM_EN**	**ACCDET_CMP_PWM_EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	ACCDET_EINT_PWM_EN	**Enables PWM of ACCDET EINT unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

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0F4C **ACCDET_CON3** **ACCDET Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH+1)Hz

0F4E **ACCDET_CON4** **ACCDET Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH+1)/(PWM_WIDTH+1) PWM output high time = (PWM_THRESH+1)/32,768 sec

0F50 **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

0F52 **ACCDET_CON6** **ACCDET Control Register 6** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**Debounce time control of state 0** Debounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

0F54 ACCDET_CON7 ACCDET Control Register 7 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**Debounce time control of state 1** Debounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

0F56 ACCDET_CON8 ACCDET Control Register 8 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**Debounce time control of state 2** Debounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

0F58 ACCDET_CON9 ACCDET Control Register 9 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE3	**Debounce time control of state 3** Debounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

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0F5A ACCDET_CON10 ACCDET Control Register 10 0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	Debounce time to control AUXADC when in state 0

0F5E ACCDET_CON12 ACCDET Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_IRQ_POLARITY					ACCDET_EINT_IRQ_CLR	ACCDET_NEGV_IRQ_CLR	ACCDET_IRQ_CLR						ACCDET_EINT_IRQ	ACCDET_NEGV_IRQ	ACCDET_IRQ
Type	RW					RW	RW	RW						RO	RO	RO
Reset	0					0	0	0						0	0	0

Bit(s)	Name	Description
15	ACCDET_EINT_IRQ_POLARITY	**ACCDET EINT IRQ POLARITY** 1'b0: Falling edge 1'b1: Rising edge
10	ACCDET_EINT_IRQ_CLR	**Clears ACCDET_EINT interrupt status When ACCDET_EINT interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.**
9	ACCDET_NEGV_IRQ_CLR	**Clears ACCDET_NEGV interrupt status When ACCDET_NEGV interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_NEGV design until both the interrupt status and IRQ_CLR are cleared.**
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
2	ACCDET_EINT_IRQ	**Clears ACCDET_EINT interrupt status**
1	ACCDET_NEGV_IRQ	**Clears ACCDET_NEGV interrupt status**
0	ACCDET_IRQ	**ACCDET interrupt status** Due to this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design.

0F62 ACCDET_CON14 ACCDET Control Register 14 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_A	ACCDET_C	ACCDET_V	ACCDET_M												

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	UDACCDETAUXADCSWCTRL	MP_CLK	TH_CLK	BIAS_CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_NI_AUDACCDET AUXADCSWCTRL	ACCDET to AUXADC switch control
14	ACCDET_CMP_CLK	Comparator turn-on control for accessory detection
13	ACCDET_VTH_CLK	Turns on threshold voltage for accessory detection
12	ACCDET_MBIAS_CLK	Turns on earphone bias voltage for accessory detection

0F64 ACCDET_CON 15 ACCDET Control Register 15 0061

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT_PWM_WIDTH			ACCDET_EINT_PWM_THRESH				ACCDET_EINT_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	0				

Bit(s)	Name	Description
13:12	ACCDET_EINT_PWM_WIDTH	**ACCDET EINT PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT_PWM_THRESH	**ACCDET EINT PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:4	ACCDET_EINT_DEBOUNCE	**ACCDET EINT debounce time** 3'b000: 1ms 3'b001: 2ms 3'b010: 4ms 3'b011: 8ms 3'b100: 16ms 3'b101: 32ms 3'b110: 256ms 3'b111: 512ms

0F66 ACCDET_CON ACCDET Control Register 16 0161

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_PWM_RISE_DELAY										ACCDET_EINT_PWM_FALL_DELAY	ACCDET_NEGV_THRESH				
Type	RW										RW	RW				
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1

Bit(s)	Name	Description
15:6	ACCDET_EINT_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.
4:0	ACCDET_NEGV_THRESH	**ACCDET NVG debounce threshold** 5'd0: 1/32 5'd1: 2/32 5'd2: 3/32 5'd3: 4/32 5'dN: (N+1)/32

0F6A **ACCDET_CON19** **ACCDET Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINTCMPEN	AD_EINTCMPOUT	AD_NVDETECTOUT													
Type	RO	RO	RO													
Reset	0	0	0													

Bit(s)	Name	Description
15	DA_NI_EINTCMPEN	
14	AD_EINTCMPOUT	
13	AD_NVDETECTOUT	

0F78 **CHR_CON0** **Charger Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET		RGS_CHRDET	RG_NORM_CHR_EN	RG_CSDAC_EN		RGS_CHRLDO_DET	RG_VCDT_HV_EN
Type									RO		RO	RW	RW		RO	RW
Reset									0		0	0	0		0	1

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Bit(s)	Name	Description
7	RGS_VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce).** 0: charge-in voltage < VCDT_HV_VTH 1:charge-in voltage > VCDT_HV_VTH
5	RGS_CHRDET	**Charger-in detect.** 0: No valid charger detected 1: Valid charger detected
4	RG_NORM_CHR_EN	**Charger enable setting which will gate CSDAC_EN, PCHR_AUTO and HWCV_EN** 0: Disable charger 1: Enable charger
3	RG_CSDAC_EN	**Enables CS DAC** 0: Disable CS DAC 1: Enable CS DAC
1	RGS_CHR_LDO_DET	**Detects charger LDO** If not detected, pulse charger cannot work. 0: Invalid charger LDO 1: Valid charger LDO
0	RG_VCDT_HV_EN	**Enables ChargerIn HV detection** 0: Disable 1: Enable

0F7A **CHR_CON1** **Charger Control Register 1** **00F2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH				RG_VCDT_LV_VTH			
Type									RW				RW			
Reset									1	1	1	1	0	0	1	0

Bit(s)	Name	Description
7:4	RG_VCDT_HV_VTH	**ChargerIn HV detection threshold** 1111: 10.5V 1110: 9.5V 1101: 8.5V 1100: 7.5V 1011: 7V 1010: 6.5V 1001: 6V 1000: 4.45V 0111: 4.4V 0110: 4.35V 0101: 4.3V 0100: 4.25V 0011: 4.2V 0010: 4.15V 0001: 4.1V 0000: 4V
3:0	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold** 1111: 10.5V 1110: 9.5V 1101: 8.5V 1100: 7.5V 1011: 7V 1010: 6.5V

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Bit(s)	Name	Description
		1001: 6V 1000: 4.45V 0111: 4.4V 0110: 4.35V 0101: 4.3V 0100: 4.25V 0011: 4.2V 0010: 4.15V 0001: 4.1V 0000: 4V

0F7C CHR_CON2 Charger Control Register 2 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VBAT_CC_DET	RGS_VBAT_CV_DET	RGS_CS_DET		RG_CS_EN	RG_VBAT_CC_EN	RG_VBAT_CV_EN	
Type									RO	RO	RO		RW	RW	RW	
Reset									0	0	0		0	1	0	

Bit(s)	Name	Description
7	RGS_VBAT_CC_DET	**VBAT voltage detection for CC** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6	RGS_VBAT_CV_DET	**VBAT voltage detection for CV** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5	RGS_CS_DET	**Current sense voltage detection** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3	RG_CS_EN	**Enables current sense voltage detection comparator** 0: Disable 1: Enable
2	RG_VBAT_CC_EN	**Enables battery CC detection** 0: Disable 1: Enable
1	RG_VBAT_CV_EN	**Enables battery CV detection** 0: Disable 1: Enable

0F7E CHR_CON3 Charger Control Register 3 00CF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VBAT_CC_VTH		RG_VBAT_NORM_CV_VTH					
Type									RW		RW					
Reset									1	1	0	0	1	1	1	1

Bit(s)	Name	Description
7:6	RG_VBAT_CC_VTH	**Battery CC dection threshold**

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Bit(s)	Name	Description
		00: 3.3V 01: 3.35V 10: 3.4V 11: 3.45V (default)
5:0	RG_VBAT_NORM_CV_VTH	**Battery CV dection threshold trimming option** Default 4.2V. This register is used for FT CV threshold trimming and not for customer's fine-tuning (pchr_dig should invert MSB bit; otherwise, BC1.1 2.2V threshold will be wrong.) 000000~000011: 3.5V, 3.6V, 3.7V, 3.8V 000100~000111: 3.85V, 3.9V, 4V, 4.05V 001000~001011: 4.1V, 4.125V, 4.1375v, 4.15V 001100~001111: 4.1625V, 4.175V, 4.1875V, 4.2V (default) 010000~010011: 4.2125V, 4.225V, 4.2375V, 4.25V 010100~010111: 4.2625V, 4.275V, 4.2875V, 4.3V 011000~011011: 4.3125V, 4.325V, 4.3375V, 4.35V 011100~011111: 4.3625V, 4.375V, 4.3875V, 4.4V 100000~100011: 4.4125V, 4.425V, 4.4375V, 4.45V 100100~100111: 4.4625V, 4.475V, 4.4875V, 4.5V 101000: 4.6V 111111: 2.2V (BC1.1)

0F80 CHR_CON4 Charger Control Register 4 000F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_NORM_CS_VTH			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	RG_NORM_CS_VTH	**Current sense voltage detection threshold @ Rcs=0.2ohm** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA (usbdl) 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA

0F84 CHR_CON6 Charger Control Register 6 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VBAT_OV_DET	RG_VBAT_OV_DEG	RG_VBAT_OV_VTH				RG_VBAT_OV_EN
Type										RO	RW	RW				RW

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset										0	0	0	0	0	1	1

Bit(s)	Name	Description
6	RGS_VBAT_OV_DET	**Detects VBAT_OV voltage** 0: VBAT voltage < VBAT_OV_VTH 1: VBAT voltage > VBAT_OV_VTH
5	RG_VBAT_OV_DEG	**Enables VBAT OV voltage detection deglitch** 0: No debounce 1: Debounce one cycle (1us)
4:1	RG_VBAT_OV_VTH	**Battery over-voltage detection threshold** 0000: 3.900V 0001: 4.200V (default) 0010: 4.300V 0011: 4.400V 0100: 4.450V 0101: 4.500V 0110: 4.600V 0111: 4.700V 1000: 3.800V
0	RG_VBAT_OV_EN	**Battery over-voltage for driving protection** 0: Disable 1: Enable

0F86 CHR_CON7 Charger Control Register 7 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_BATON_TDET_EN**						**BATON_TDET_EN**	**RG_BATON_HT_EN_RSV0**	**RG_BATON_EN**
Type								RW						RW	RW	RW
Reset								0						0	0	1

Bit(s)	Name	Description
8	RG_BATON_TDET_EN	**BATON temperature detection enable via AUXADC (gated by CHR_LDO_DET to default 0 in analog domain)** SW should enable AUXADC reference buffer before enabling this switch. This RG is also used to enable external SWCHR BATON detection. 0: Disable temperature detection related TREF power switch 1: Enable temperature detection related TREF power switch
2	BATON_TDET_EN	0: N/A 1: Enable BATON temperature detection
1	RG_BATON_HT_EN_RSV0	**Detects Battery-On HW high temperature** 0: Disable 1: Enable
0	RG_BATON_EN	**Enable BATON battery detection comparator (gated by CHR_LDO_DET to default 1 in analog domain)** 0: Disable 1: Enable (Default)

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0F8A CHR_CON9 Charger Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_FRC_CSVTH_USBDL
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_FRC_CSVTH_USBDL	**Forces CS DAC detection threshold to maximum in USB download mode** 0: CS_VTH=450mA in USBDL mode 1: CS_VTH=1600mA in USBDL mode

0F8C CHR_CON10 Charger Control Register 10 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_OTG_BVALID_DET	RG_OTG_BVALID_EN					
Type										RO	RW					
Reset										0	1					

Bit(s)	Name	Description
6	RGS_OTG_BVALID_DET	**Indicates if the session for B-peripheral is valid (0.8V<Vth<4V)** Here VBUS is connected to CHRIN. 0: Vbus < 0.8V 1: Vbus > 4V
5	RG_OTG_BVALID_EN	**Enables OTG BValid detection** 0: Disable 1: Enable

0F92 CHR_CON13 Charger Control Register 13 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_CHRWDT_WR				RG_CHRWDT_EN	RG_CHRWDT_TD			
Type								RW				RW	RW			
Reset								0				1	0	0	0	0

Bit(s)	Name	Description
8	RG_CHRWDT_WR	**Resets charger watchdog timer and updates CHRWDT_TD** 0: Reset inactive 1: Reset active and CHRWDT_TD updated to PCHR_DIG
4	RG_CHRWDT_EN	**Enables setting for charger watchdog timer** Note: UVLO don't care this bit and will time out after 3000s. PCHR_TESTMODE can force to control watchdog enable by using this bit.

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Bit(s)	Name	Description
		0: Disable 1: Enable if (CHR_EN(@CHR_CON0) = 1)
3:0	RG_CHRWDT_TD	**Time constant setting for charger watchdog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec 4: 128 sec 5: 256 sec 6: 512 sec 7: 1024 sec 8~15: 3000 sec

0F96 CHR_CON15 Charger Control Register 15 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RGS_CHRWDT_OUT**	**RG_CHRWDT_FLAG_WR**	**RG_CHRWDT_INT_EN**
Type														RO	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	RGS_CHRWDT_OUT	**Timeout flag for charger watchdog timer** Read: 0: No timeout status 1: Timeout status asserted
1	RG_CHRWDT_FLAG_WR	**Clears timeout flag for charger watchdog timer** Read: 0: N/A (when RGS_CHRWDT_OUT=0) 1: Clear timeout flag when RGS_CHRWDT_OUT=1
0	RG_CHRWDT_INT_EN	**Interrupt enable setting for charger watchdog timer** 0: Disable 1: Enable

0F98 CHR_CON16 Charger Control Register 16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_ADCIN_CHR_EN**	**RG_ADCIN_VSEN_EN**	**RG_ADCIN_VBAT_EN**	**RG_ADCIN_VSEN_EXT_BATON_EN**	**RG_ADCIN_VSEN_MUX_EN**					**RG_USBDL_SET**	**RG_USBDL_RST**		
Type				RW	RW	RW	RW	RW					RW	RW		
Reset				0	0	0	0	0					0	0		

Bit(s)	Name	Description
12	RG_ADCIN_CHR_EN	**Enables AUXADC input source for CHR** 0: Disable

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Bit(s)	Name	Description
		1: Enable
11	RG_ADCIN_VSEN_EN	**Enables AUXADC input source for VSEN** 0: Disable 1: Enable
10	RG_ADCIN_VBAT_EN	**Enables AUXADC input source for VBAT** 0: Disable 1: Enable
9	RG_ADCIN_VSEN_EXT_BATON_EN	**Enables AUXADC input source for external source to be switched to AUXADC's Ch3** 0: Disable 1: Enable
8	RG_ADCIN_VSEN_MUX_EN	**Enables AUXADC input source for VSEN to be switched to VBAT's divider** 0: Disable 1: Enable
3	RG_USBDL_SET	**USBDL_MODE software set control** 0: No effect 1: Force to enter USBDL mode
2	RG_USBDL_RST	**USBDL_MODE software reset control** 0: No effect 1: Force to leave USBDL mode (priority is lower than USBDL_DET)

0F9A CHR_CON17 Charger Control Register 17 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_UVLO_VH_LAT			RG_UVLO_VTHL				
Type									RW			RW				
Reset									0			0	0	1	0	0

Bit(s)	Name	Description
7	RG_UVLO_VH_LAT	**UVLO VH latch signal** 0: Disable 1: Enable
4:0	RG_UVLO_VTHL	**Selects UVLO low threshold** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V

0F9C CHR_CON18 Charger Control Register 18 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_LBAT_INT_VTH				
Type												RW				

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Reset											0	0	0	1	1

Bit(s)	Name	Description
4:0	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V 01001: 2.95V 01010: 3.0V 01011: 3.05V 01100: 3.1V 01101: 3.15V 01110: 3.2V 01111: 3.25V 10000: 3.3V 10001: 3.35V 10010: 3.4V

0F9E CHR_CON19 Charger Control Register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BGR_UNCHOP	RG_BGR_UNCHOP_PH		RG_BGR_RSEL		
Type											RW	RW		RW		
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	RG_BGR_UNCHOP	**BGR unchop mode** 0: Chop mode 1: Unchop mode
4	RG_BGR_UNCHOP_PH	**Selects BGR unchop mode phase** 0: Select phase 0 path in unchop mode 1: Select phase 1 path in unchop mode
2:0	RG_BGR_RSEL	**Selects BGR resistor (R0 = R1)** R2=85K, and VBG=(R0/R2)*dVBE+VBE 0: c0, 780K (default) 1: c1, 820K 2: c2, 860K 3: c3, 900K 4: cm4, 620K 5: cm3, 660K 6: cm2, 700K 7: cm1, 740K

0FA0 CHR_CON20 Charger Control Register 20 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_BC11_CMP_OUT				RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL
Type									RO				RW		RW	RW
Reset									0				0	0	0	0

Bit(s)	Name	Description
7	RGS_BC11_CMP_OUT	**Detects comparison result of BC11 charger** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
3:2	RG_BC11_VSRC_EN	**BC11 voltage source** Set VDP_SRC = 0.6V 0: Disable voltage 1: Enable voltage source to DM 2: Enable voltage source to DP 3: Forbidden
1	RG_BC11_RST	**Resets BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG.
0	RG_BC11_BB_CTRL	**Forces BC11 charger detection controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode) 1: BC11 detection by baseband (software mode)

0FA2 **CHR_CON21** **Charger Control Register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type								RW	RW		RW		RW		RW	
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RG_BC11_BIAS_EN	**Enables BC11 detection bias circuit** 0: Disable 1: Enable
7:6	RG_BC11_IPU_EN	**Enables BC11 7~15uA pull-up current** 0: Disable pull-up current 1: Enable pull-up current to DM 2: Enable pull-up current to DP 3: Forbidden
5:4	RG_BC11_IPD_EN	**BC11 50~150uA pull-down current** 0: Disable pull-down current 1: Enable pull-down current to DM 2: Enable pull-down current to DP 3: Forbidden
3:2	RG_BC11_CMP_EN	**BC11 comparator connection** 0: Disable comparator 1: Enable comparator to DM 2: Enable comparator to DP 3: Forbidden

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Bit(s)	Name	Description
1:0	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.325V 1: VREF_VTH=1.2V 2, 3: VREF_VTH=2.6V

0FA6 CHR_CON23 Charger Control Register 23 0024

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP				RG_CSDAC_DLY		
Type										RW				RW		
Reset										0	1	0		1	0	0

Bit(s)	Name	Description
6:4	RG_CSDAC_STP	**Current DAC output step timer** 1/1/2/3/4/5/6/7 code/ per-step
2:0	RG_CSDAC_DLY	**Current DAC output detection delay control** 16/32/64/128/256/512/1024/2048us (512us default, reused in HW CV mode)

0FA8 CHR_CON24 Charger Control Register 24 0044

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CHRIND_DIMMING	RG_CHRIND_ON	RG_LOW_ICH_DB					
Type									RW	RW	RW					
Reset									0	1	0	0	0	1	0	0

Bit(s)	Name	Description
7	RG_CHRIND_DIMMING	**Enables pre-charge indicator dimming** 0: Disable 1: Enable
6	RG_CHRIND_ON	**Pre-charge indicator on (gated by CHR_LDO_DET to default 0 in analog domain)** 0: Disable indicator 1: Enable indicator
5:0	RG_LOW_ICH_DB	**Plug-out HW detection debounce time (base=16ms)** Debounce time: Code*16ms

0FAA CHR_CON25 Charger Control Register 25 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ULC_DET_EN	RG_HWCV_EN		RG_TRACKING_EN		RG_CSDAC_MODE	RG_VCDT_MODE	RG_CV_MODE
Type									RW	RW		RW		RW	RW	RW
Reset									0	0		1		0	0	0

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Bit(s)	Name	Description
7	RG_ULC_DET_EN	**Enables charger plug-out auto detection** This fuction should be applied with RG_HWCV_EN=1. 0: Disable 1: Enable
6	RG_HWCV_EN	**Enables hardware CV current tracking** 0: Disable 1: Enable
4	RG_TRACKING_EN	**0: Current calibration uses CS_VTH[n] and CS_VTH[n-1] as high/low threshold.** 1: Current calibration uses CS_VTH[n] and LTH as high/low threshold.
2	RG_CSDAC_MODE	**0: If not entering CC, charging is AUTO mode.** 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode).
1	RG_VCDT_MODE	**Selects charger detection mode** 0: Charger detection can only be active in off state. 1: Charger detection is active in both on and off state.
0	RG_CV_MODE	**Selects battery CV detection mode** 0: CV detection can only be active in off state. 1: CV detection is active in both on and off state.

0FB4 CHR_CON30 Charger Control Register 30 0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DAC_USBDL_MAX									
Type							RW									
Reset							0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
9:0	RG_DAC_USBDL_MAX	**USBDL maximum current setting** Default: 85 => 0001010101

0FB6 CHR_CON31 Charger Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PCHR_CM_VDEC_STATUS				RG_CM_VDEC_TRIG
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VDEC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done.
0	RG_CM_VDEC_TRIG	**Automatic current procedure trigger in adaptor output voltage**

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Bit(s)	Name	Description
		decrement communication mode 0: No effect 1: Trigger automatic current procedure in adaptor output voltage decrement communication mode

0FB8 CHR_CON32 Charger Control Register 32 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**PCHR_CM_VINC_STATUS**				**RG_CM_VINC_TRIG**
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VINC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done.
0	RG_CM_VINC_TRIG	**Automatic current procedure trigger in adaptor output voltage increment communication mode** 0: No effect 1: Trigger automatic current procedure in adaptor output voltage increment communication mode

0FBA CHR_CON33 Charger Control Register 33 1D1D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RG_CM_VDEC_HPRD2**								**RG_CM_VDEC_HPRD1**					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD2	**2nd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD1	**1st high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms

0FBC CHR_CON34 Charger Control Register 34 091D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RG_CM_VDEC_HPRD4**								**RG_CM_VDEC_HPRD3**					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD4	**4th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD3	**3rd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms

0FBE CHR_CON35 Charger Control Register 35 3109

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD6								RG_CM_VDEC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD6	**6th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD5	**5th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms

0FC0 CHR_CON36 Charger Control Register 36 0909

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD2								RG_CM_VINC_HPRD1					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD2	**2nd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VINC_HPRD1	**1st high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

0FC2 CHR_CON37 Charger Control Register 37 1D1D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD4								RG_CM_VINC_HPRD3					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD4	**4th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

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Bit(s)	Name	Description
5:0	RG_CM_VINC_HPRD3	**3rd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

0FC4 CHR_CON38 Charger Control Register 38 311D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD6								RG_CM_VINC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD6	**6th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VINC_HPRD5	**5th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

0FC6 CHR_CON39 Charger Control Register 39 0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_CM_LPRD					
Type											RW					
Reset											0	0	1	0	0	1

Bit(s)	Name	Description
5:0	RG_CM_LPRD	**Low pulse width in communication mode** Low pulse width = (Setting+1)*10ms

0FC8 CHR_CON40 Charger Control Register 40 00AF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CM_CS_VTHH				RG_CM_CS_VTHL			
Type									RW				RW			
Reset									1	0	1	0	1	1	1	1

Bit(s)	Name	Description
7:4	RG_CM_CS_VTHH	**Current sense detection high threshold in communication mode** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA

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Bit(s)	Name	Description
		0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA
3:0	RG_CM_CS_VTHL	**Current sense detection low threshold in communication mode** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA

0FCA **CHR_CON41** **Charger Control Register 41** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RSV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_PCHR_RSV	Reserved

0FCC **CHR_CON42** **Charger Control Register 42** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ENVTEM_EN	RG_ENVTEM_D
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_ENVTEM_EN	**Blocks CHR_DET signal to start_up** 0: N/A 1: Enable write
0	RG_ENVTEM_D	**Blocks CHR_DET signal to start_up** 0: Does not block 1: Block

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0FD0 CHR_CON43 Charger Control Register 43 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CM_VINC_INT_EN		RG_CM_VDEC_INT_EN									
Type					RW		RW									
Reset					0		0									

Bit(s)	Name	Description
11	RG_CM_VINC_INT_EN	Enables Pump Express VDEC INT
9	RG_CM_VDEC_INT_EN	Enables Pump Express VDEC INT

0FD2 CHR_CON44 Charger Control Register 44 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RGS_BATON_UNDET	RG_QI_BATON_LT_EN
Type															RO	RW
Reset															0	1

Bit(s)	Name	Description
1	RGS_BATON_UNDET	**Battery-On undetected** 0: Detected 1: Not detected
0	RG_QI_BATON_LT_EN	

0FD8 CHR_CON47 Charger Control Register 47 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_BC11_ACA_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_BC11_ACA_EN	Enables BC11 ACA detection

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0FDA CHR_CON48 Charger Control Register 48 0C08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RGS_BC11_ACA_OTG_DET	RGS_BC11_ID_GND	RGS_BC11_ID_C	RGS_BC11_ID_B	RGS_BC11_ID_A	RGS_BC11_ID_FLOAT	RG_VCDT_TRIM			
Type							RO	RO	RO	RO	RO	RO	RW			
Reset							0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
9	RGS_BC11_ACA_OTG_DET	Interrupt for BC11 ACA (ID_A | ID_B | ID_C | ID_GND)
8	RGS_BC11_ID_GND	Shorts BC11 ID pin to GND
7	RGS_BC11_ID_C	BC11 ID pin C condition
6	RGS_BC11_ID_B	BC11 ID pin B condition
5	RGS_BC11_ID_A	BC11 ID pin A condition
4	RGS_BC11_ID_FLOAT	BC11 ID pin floating
3:0	RG_VCDT_TRIM	Trims VCDT for 2% viration spec

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4 Application Notes

4.1 Hardware External Shutdown

The following schematic illustrates the hardware external shut-down function for MT6351 to power down when the main chip software crashes.

- Short press PWRKEY or FCHR_ENB
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14 s with < 1% accuracy
  - External reset function with source from:
    - PWRKEY and FCHR_ENB both pressed for a long period of time
    - PWERKEY pressed for a long period of time
    - FCHR_ENB pressed for a long period of time
  - Software disables watchdog counter.

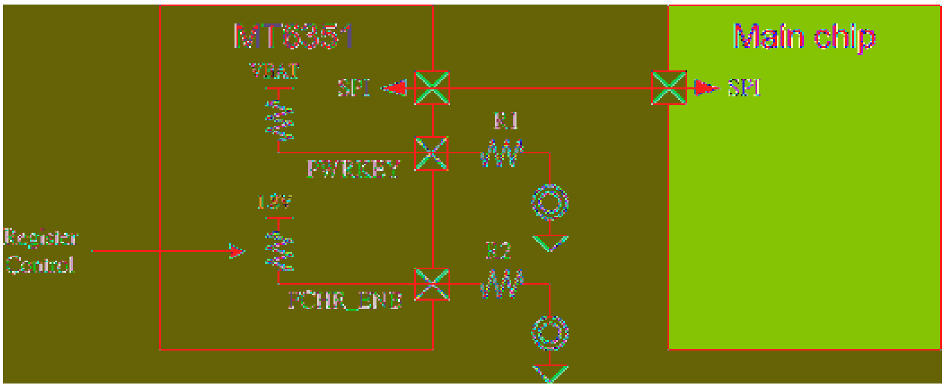

Figure 4-1. Hardware external shut-down function

4.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6351 VPA buck converters that is not used.

- Configuration for VPA not in use:
  - Connect VBAT_PA to VBAT; connect GND_PA to GND
  - VPA & VPA_FB: Floating
  - RG_VPA_EN = 0 & RG_VPA_NDIS_EN = 1 (software setting)

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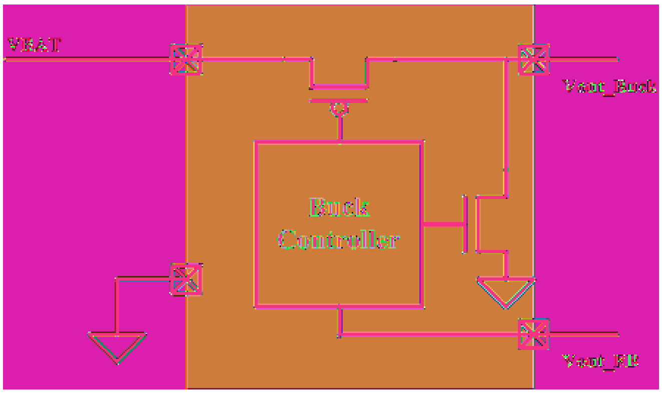

Figure 4-2. Configuration for unused DC/DC

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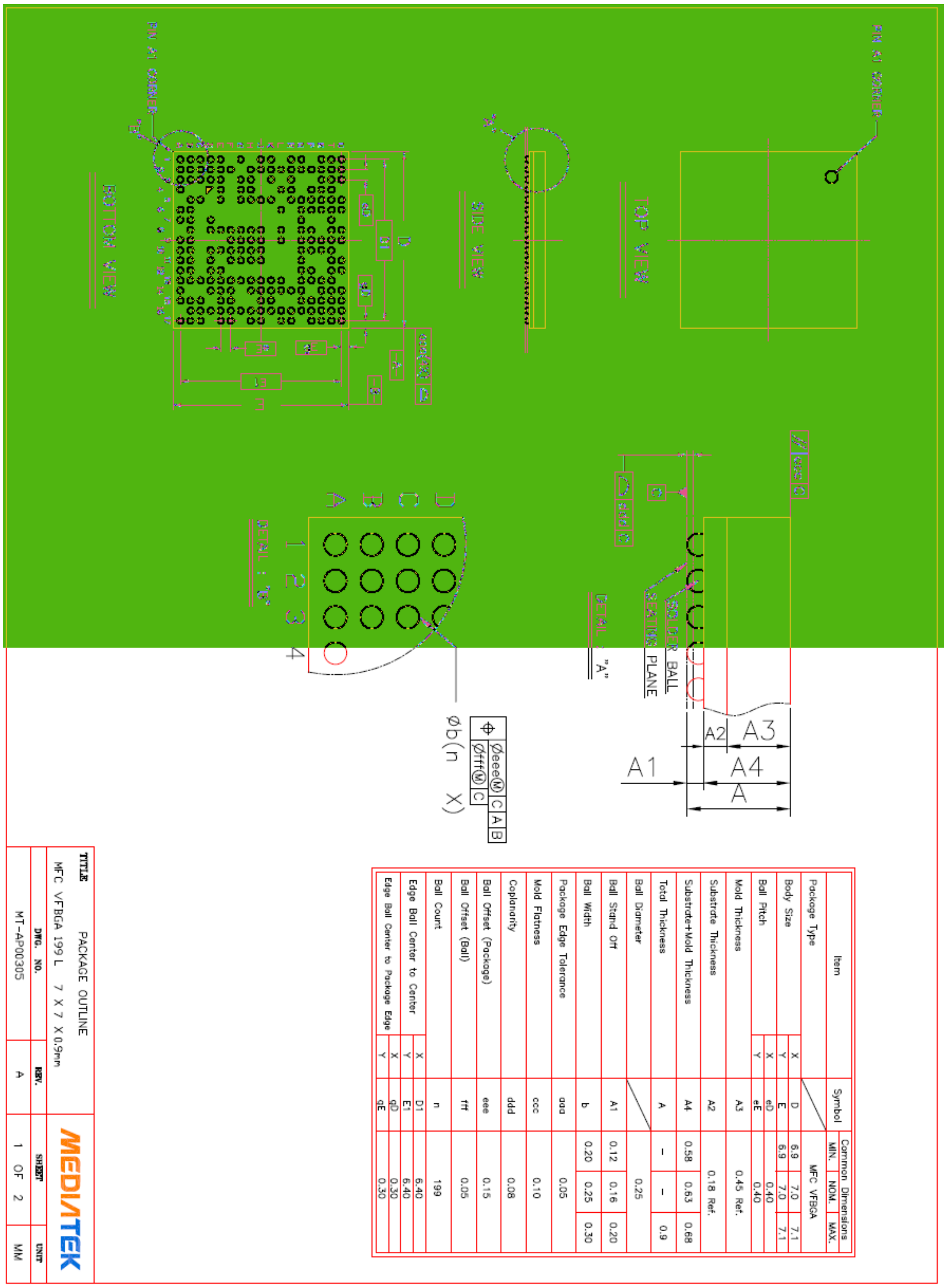
5 MT6351 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	6.9	7.0	7.1
	Y	E	6.9	7.0	7.1
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.18 Ref.	
Substrate+Mold Thickness		A4	0.58	0.63	0.68
Total Thickness		A	–	–	0.9
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		199	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.40	
Edge Ball Center to Package Edge	X	qD		0.30	
	Y	qE		0.30	

Figure 5-1. Package dimension

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Appendix

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